POWER SWITCH

By
Pierre Aloisi

Power Products
Senior Applications Engineer
Motorola Toulouse

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Preface

In this work, it was my intent to try to answer some of many questions posed by power circuit designer about power semiconductors. A great deal of the information in this book is a direct result of the enormous amount of work and analysis conducted in the power products laboratory at Motorola, Toulouse, over the past five years.

In order to accomplish this task, i put together some of the latest developments in solid state physics as it applies to power components. In my opinion knowledge of new technologies is a key element in understanding the trade-offs in performance of the many devices that are available in todays market place. These technology developments form the base for the first section of the book. The second section, consisting of chapters 2 and 3, is a brief study of the various types of power semiconductor switches that are available today and how they interact with their environment. In the last section, we look at various factors that should be considered before chosing the proper power switch for a specific application.

A second book is planned for the near future which will feature the various applications for power switches.

Finally, I would like to thank all those anonymous inventors who have allowed me, through their pertinent questions, to discover so many things about power electronics.

I would also like to mention all the European Universities, Henri Foch, Pierre Rossel, Tore Underland... and their research teams who enlightened me with their contributions.

I wish to extend my thanks to all the engineers in the Motorola power semiconductor group, Phoenix and Toulouse for their help, their suggestions and advice.

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Physical properties of power devices

1. Thermal resistance

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A-1. Introduction

The instantaneous temperature of a semiconductor junction is difficult to determine and is not normally used despite of its importance for reliable operation. For high power components this temperature can change very quickly, up to 10^6°C/sec, so that the mean temperature of the junction is entirely inadequate for measuring the safety margin of a given function.

A technique using analysis of thermal and electrical conduction in an R.C. network has been perfected by W.E. Newell (1) and A. Fillatre (5).

This very practical and comprehensive method may be applied to a wide variety of situations.

It makes use of a graphic tool to evaluate the rise in temperature of a given material.

A-2. Definition of terms and units

Table 1-1

Descriptions	Symbols	Units	Electric analog symbol
Increase in temperature	Δt	°C	V
Power waste	P	W	I
Thermal resistance	$R\theta$	°C/W	R
Thermal capacity	$C\theta$	J/°C	C
Thermal impedance	$Z\theta$	°C/W	Zin
Transient thermal impedance Thermal response or step function	$r(t)Z\Theta$	°C/W	V/Is
Thermal conductivity	K	W/cm.°C	
Material density	ρ	g/cm³	
Specific heat	C	J/g.°C	
Material thickness	e	cm	

Thermal equations

Thermal resistance : $R\theta = \frac{e}{k}$

Thermal capacity : $C\theta = \rho C\ (e\,s) = \rho C$ Volume = C. weight

Table 1-2 – Thermal constants of electronic materials

	Steel	Aluminium	Copper	Silicon	Molybdenum	Eutectic	Pb Ag In	Mica epoxy	AL2 03 alumine	Calme air
Density ρ	7.75	2.70	8.85	2.33	10.22		11	3	3.7	$13\ 10^{-4}$
Thermal capacity C = J/g°C	.45	.90	.39	.75	.27	.3	.13	.84	.85	1
Thermal conductivity K = W/cm.°C	.46	2.05	3.85	.84	1.46	2.2	.36	.003	.37	$3\ 10^{-4}$

A-3. Hypothesis

If a solid, semi-infinite center, unidimentional object is exposed to P amount of power the temperature rise at the surface of the solid object is given by:

$$\Delta T\ (t) = \left[\frac{4}{\pi}\ \frac{t}{k\rho c}\right]^{\frac{1}{2}} P \qquad (1)$$

t is measured from the moment that P is applied.

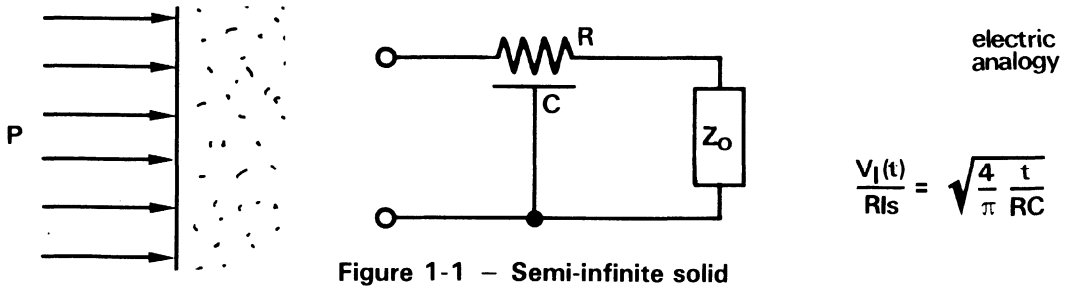


Figure 1-1 – Semi-infinite solid

For plates of finite thickness e, formula (1) may be used for "short duration pulses" (see later) otherwise 2 possible cases exist for the equilibrium condition.

A-3.1. Isothermic boundary surface, the temperature rise $\Delta T(t)$ asymptotically approaches the equilibrium state and can be expressed as follows:

$$\Delta T\ (t) = \frac{e}{k} P \qquad (2)$$

with $e/k = R\Theta$ (thermal resistance of material).

An analogy can be made to an electrical circuit with a distributed impedance and a short circuit.

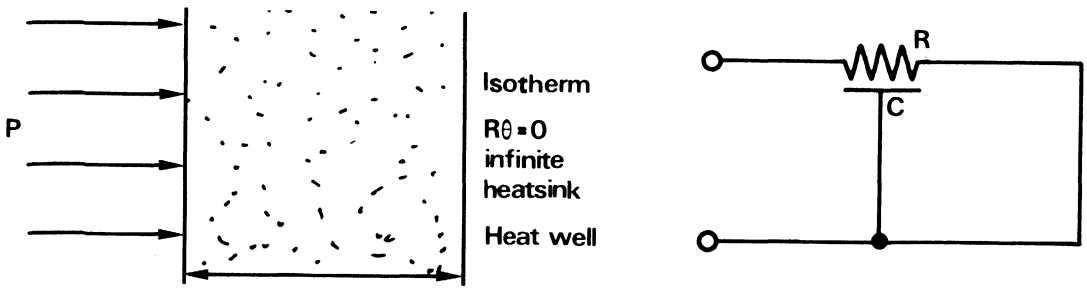


Figure 1-2 – Solid with finite e thickness and infinite heatsink.

A-3.2. ADIABATIC BOUNDARY SURFACE

We obtain: for large value of t $\Delta T(t) = \frac{t}{\rho C e} P$ (3)

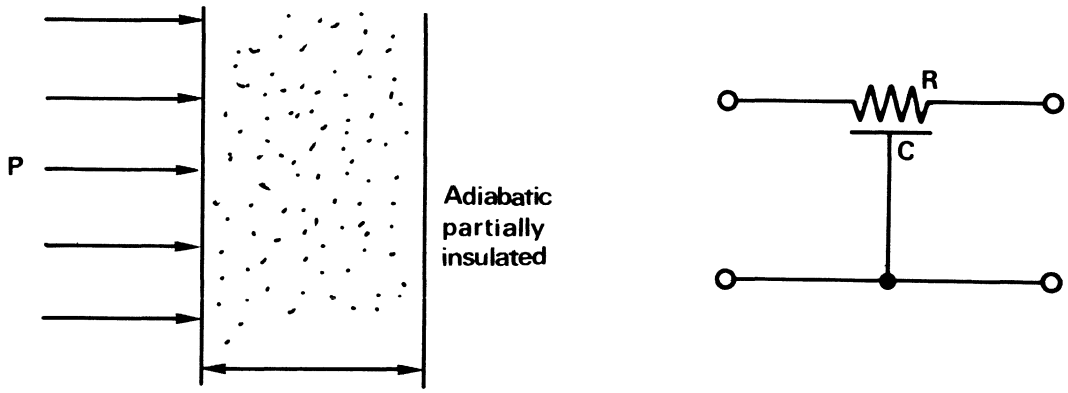


Figure 1-3 – Solid with finite e thickness and mounted on an insulated surface

A-4. Graphic representation of asymptotes in logarithmic co-ordinates

If V1(t) / RIs is represented in terms of time t/Rc we get for each of the 3 study cases:
- semi-infinite solid line terminated on its characteristic impedance
- solid terminated on a heat sink, line short circuited
- solid terminated on a thermal insulator, open line

The following asymptotes:

The intersections of the asymptotes by temperature rises in terms of time defines the "Thermal Transient Times".

In second case: isotherm, we have: $\tau 1 = \frac{\pi}{4} \frac{\rho c}{k} e^2$ (4)

In the third case: adiabatic, we have: $\tau 2 = \frac{4}{\pi} \frac{\rho c}{k} e^2$ (5)

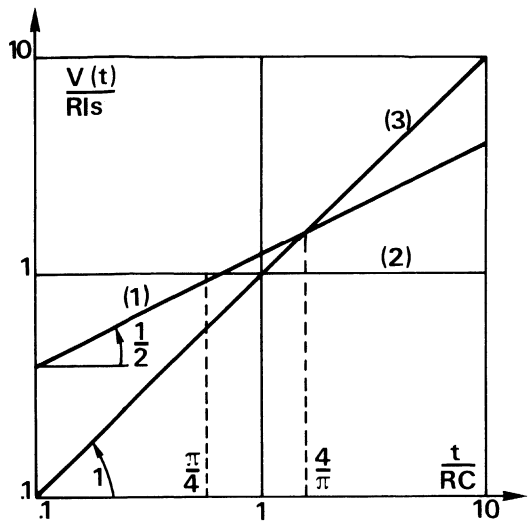


Figure 1-4 – Representation of asymptomes for equivalent electrical circuits

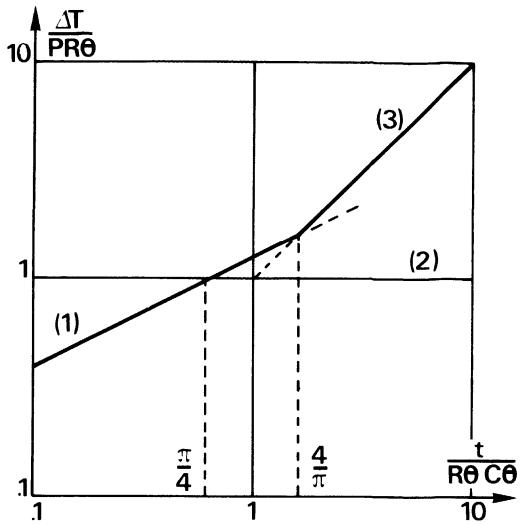


Figure 1-5 – Thermal asymptotes

If t $< \tau 1$ and the material is semi-infinite formula (1) is used, if t $> \tau_1$ and the material is connected to an infinite heat sink formula (2) is used, if t $> \tau 2$ and the material is connected to an insulating surface formula (3) is used.

A-5. Multi layer system

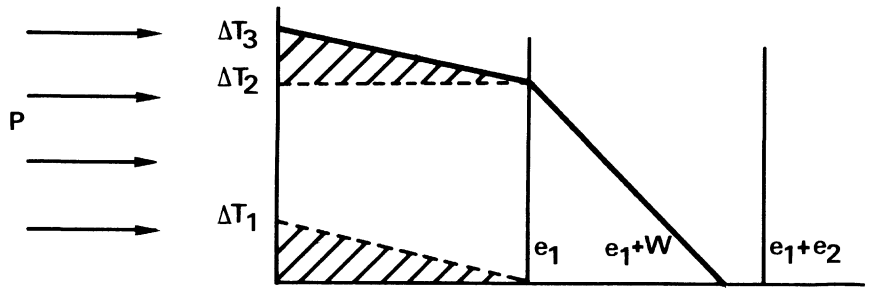


Figure 1-6 – Multi layer system

If a material has a constant temperature gradient, then the quantity of heat introduced during time t is equal to: $Q = Pt$.

This quantity is proportional to the area of the bottom shaded triangle in Figure 1-6.

$$\alpha\left(\frac{1}{2}\,\Delta T_1\, e_1\right) = Pt$$

The α equivalent factor to make the formula homogeneous is equal to $\rho_1\ C_1$ giving:

$$\frac{1}{2}\,\Delta T_1 \rho_1 C_1 e_1 = Pt$$

This can also be written for a stabilized linear system on a heatsink, as: $\Delta T_1 = \frac{P}{k_1} e_1$ by eliminating e_1 we get: $\Delta T_1^2 = \frac{2t}{k_1 \rho_1 c_1} P2$ or $\Delta T_1 = \left[\frac{2t}{k_1 \rho c_1}\right]^{1/2} P$ (6)

The thermal transient time is defined for $\tau = t$ when the propagation front reaches the heat sink as: $T = \tau = \frac{1}{2} \frac{\Delta T_1}{P} \rho_1 c_1 e_1 = \frac{1}{2} \frac{\rho_1 c_1}{k_1} e_1^2$ (7)

If there is an e_2 non isothermic layer, it may be written as: $\Delta T_3 = \Delta T_2 + \Delta T_1 = \Delta T_2 + \frac{P}{k_1} e_1$ with $\Delta T_2 = \frac{P}{k_2} W$

The heat quantity introduced is at time $t > \tau 1$

area of second layer triangle $\frac{1}{2} \Delta T_2 w$

+ area of rectangle, first layer $\Delta T_2 e_1$

+ area of triangle, first layer $\frac{1}{2} \Delta T_1 e_1$

So that: $Pt = \frac{1}{2} \rho_2 C_2 W \Delta T_2 + \rho_1 c_1 e_1 \Delta T_2 + \frac{1}{2} \Delta T_1 e_1 \rho_1 c_1$

If we write τ (1 + 2) as the first and second layer thermal transient time, we get $W = e_2$, ie: $(\frac{1}{2} \rho_2 c_2 e_2 + \rho_1 c_1 e_1) \frac{e_2}{k_2} P + \frac{1}{2} e_1 \rho_1 c_1 \frac{e_1}{k_1} P = P(\tau 1+2)$ with $\Delta T_2 = \frac{P}{k_2} e_2$, $\Delta T_1 = \frac{P}{k_1} e_1$

Therefore: $\tau 1+2 = \frac{1}{2} \frac{\rho_1 c_1}{k_1} e_1^2 + \frac{1}{2} \frac{\rho_2 c_2 e_2^2}{k_2} + \frac{\rho_1 c_1 e_1 e_2}{k_2}$ (8)

When the propagation front reaches the heat sink, we have the equilibrium state for which: $\frac{\Delta T}{P} \infty = \frac{e_1}{k_1} + \frac{e_2}{k_2}$

For a 3 layer system we would have:

$\tau 1+2+3 = \frac{1}{2} \frac{\rho 1 c 1}{k_1} e_1^2 + \frac{1}{2} \frac{\rho 2 c 2}{k_2} e_2^2 + \frac{1}{2} \frac{\rho 3 c 3}{k_3} e_3^2 + \frac{\rho_1 c_1 e_1 e_2}{k_2} + \frac{\rho_1 c_1 e_1 e_3}{k_3} + \frac{\rho_2 c_2 e_2 e_3}{k_3}$ (9)

with a heat sink, one could write $\frac{\Delta T}{P} \infty = \frac{e_1}{k_1} + \frac{e_2}{k_2} + \frac{e_3}{k_3}$ for greater accuracy and consistancy of the Newell concept, the factor $\frac{4}{\pi}$ should be substituted for the factor 2 in equations (7) (8) and (9).

In general for an i-layer system, the total transfer time on a heat sink is.

$$\tau 1 + \ldots i = \sum_o^i \left[\frac{\pi}{4} \frac{\rho i \, ci \, ei^2}{ki} + \frac{ei}{ki} \sum_o^{i-1} \rho_i \, e_i \, c_i\right] \quad (10)$$

and its preceding time is known $\tau + \ldots i\text{-}1$ one can write:

$$\tau 1 + \ldots i = \tau i + \ldots i - 1 + \frac{\pi}{4} \rho_i c_i \frac{e_i^2}{k_i} + \frac{e_i}{k_i} \sum_o^{i-1} \rho_i \, e_i \, C_i$$

To construct an asymptotic diagram representing the temperature changes a of multi-layer system with power applied you simply calculate:

1) the combined transient times:

$\tau 1,\ \tau 1+2,\ \tau 1+2+3, \ldots$

corresponding to the interfaces of the various levels.

2) the combined thermal resistances: $\frac{e_1}{k_1}, \frac{e_1}{k_1}+\frac{e_2}{k_2}, \frac{e_1}{k_1}+\frac{e_2}{k_2}+\frac{e_3}{k_3}, \ldots..$

these points define the "breakpoints" of an asymptotic diagram in logarithmic co-ordinates.

Table 1-3 – Example

	$e_{(cm)}$	e/k	$\frac{\pi}{4}\frac{\rho c}{k} e^2$ (ms)	$\frac{e_i}{k_i}\sum_{o}^{i-1} \rho_i c_i e_i$	$\Sigma\tau$
Silicon	.025	.03	1		
Molybdenum	.003	.002	.005	.1	1.105
Copper	.4	.1	110	.45+10	121.6
Aluminium	1.5	.75	2500	1000+7+40	3668

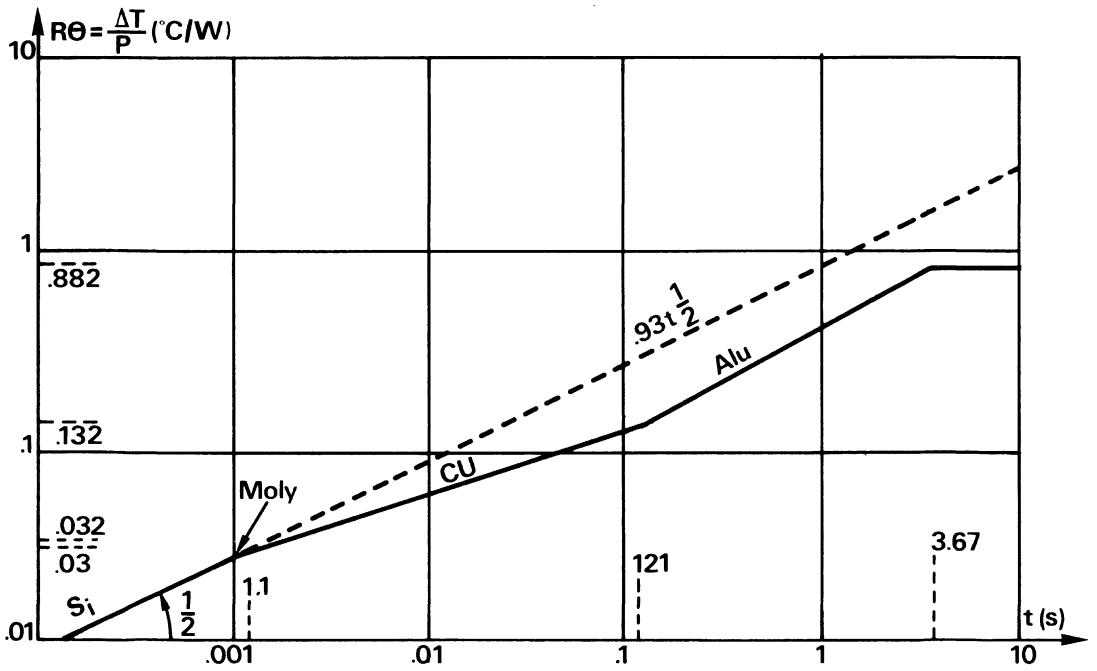


Figure 1-7 – Thermic stacking of a semiconductor

A-6. Real components

The hypothesis of the unidimensionality of heat flow is only valid if the thermal penetration is minimal relative to the lateral dimensions of the active area. A significant improvement in accuracy can be obtained by assuming that the heat flows in a "truncated cone" having a 45° angle at the top, per Figure 1-8.

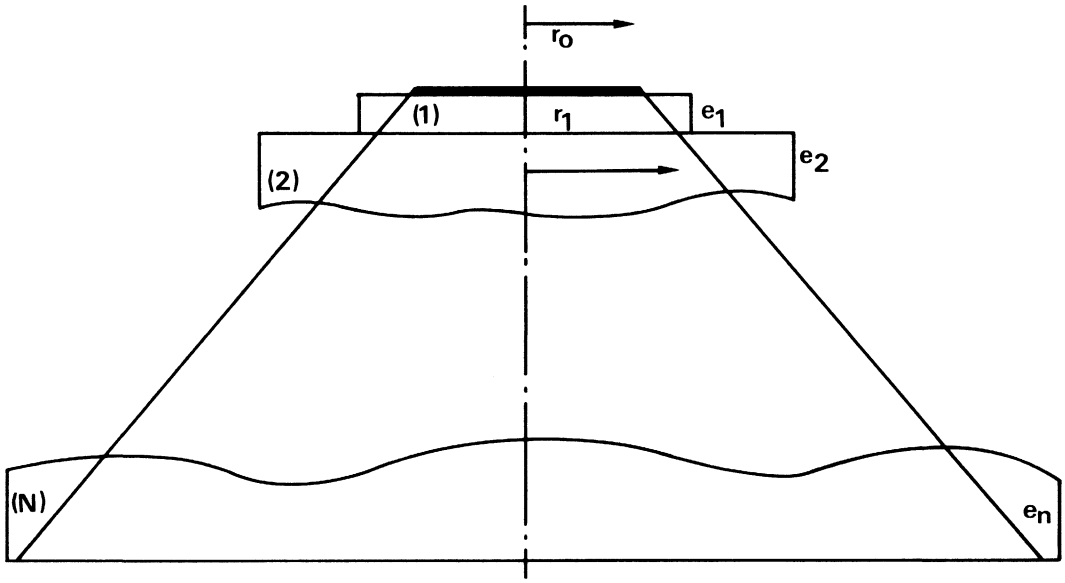


Figure 1-8 – Heat diffusion in "truncated cone"

For each layer in a multi-layer system, we can define an area S', a thermal conductivity K'I and a specific heat C'I and for any layer I we can write:

$$RTHI = \frac{1}{KI}\int_o^{eI} \frac{dx}{area} \quad \text{with Areas} = \pi\left[r_{I-1}+x\right]^2 \quad \text{for a circle}$$

$$= \left[a+2x\right] \quad \text{for a square with side a}$$

$$= (a+2x)\,(b+2x) \quad \text{for a rectangle sides a and b}$$

$$\text{so: RTHI circle} = \frac{1}{k_I \pi}\,\frac{e_I}{r_{I-1}\,(r_{i-I}+e_I)} \qquad RTHI \text{ square} = \frac{1}{k_I}\,\frac{e_I}{(a_{I-1}+2eI)\,a_{I-1}}$$

$$RTHI \text{ rectangle} = \frac{1}{k_I}\,\frac{1}{2(a_{I-1}-b_{I-1})}\,Ln\left(\frac{a_{I-1}}{b_{I-1}}\right)\left(\frac{2eI+bI-1}{2eI+aI-1}\right)$$

Equating (rI-1) for the circle to the diameter r_o of the active surface, we have:

$rI-1 = ro+e1.....+eI-1$

For the square, we have: $aI-1 = a+2e_1+2e_2 \ldots\ldots+2e_{I-1}$

The thermal conductivity K'I of the equivalent layer is:

$$RTHI = \frac{1}{k'I}\,\frac{eI}{\pi ro^2} \qquad \text{Thus K'I for me circle} = \frac{1}{RTH}\,\frac{eI}{\pi ro^2} = KI\,\frac{(ro+..eI-1)(ro+..eI)}{ro^2}$$

It follows that based on the total transient response time we have: $C'l = \frac{k'l}{kl} Cl$

or K'l square = $\frac{1}{RTH} \frac{el}{a2} = \frac{kl\,(a+2el \ldots 2el-1)\,(a+\ldots 2el)}{a^2}$

As an example, let us consider the Motorola BU208, a bipolar transistor with square active surface of $S' = 14 \times 10^{-2}$ cm².

Table 1-4

	e_{cm}	k'	$C' = \frac{k'}{k} c$	e/k's'	$R\theta$	$\frac{\pi}{4} \frac{\rho c}{k} e^2 ms$	$\frac{ei}{ki} \sum_{o}^{i-1} \rho_i c_i e_i$	τi ms
Silicon	275×10^{-4}	.95	.85	.2		1.2		1.2
Pb Ag In	40×10^{-4}	.475	.17	.17	.37	.05	.5	1.8
Copper	.15	8.5	.86	.13	.50	16.0	1.1	19
Steel	.15	4.15	2.28	.26	.76	76	44	139

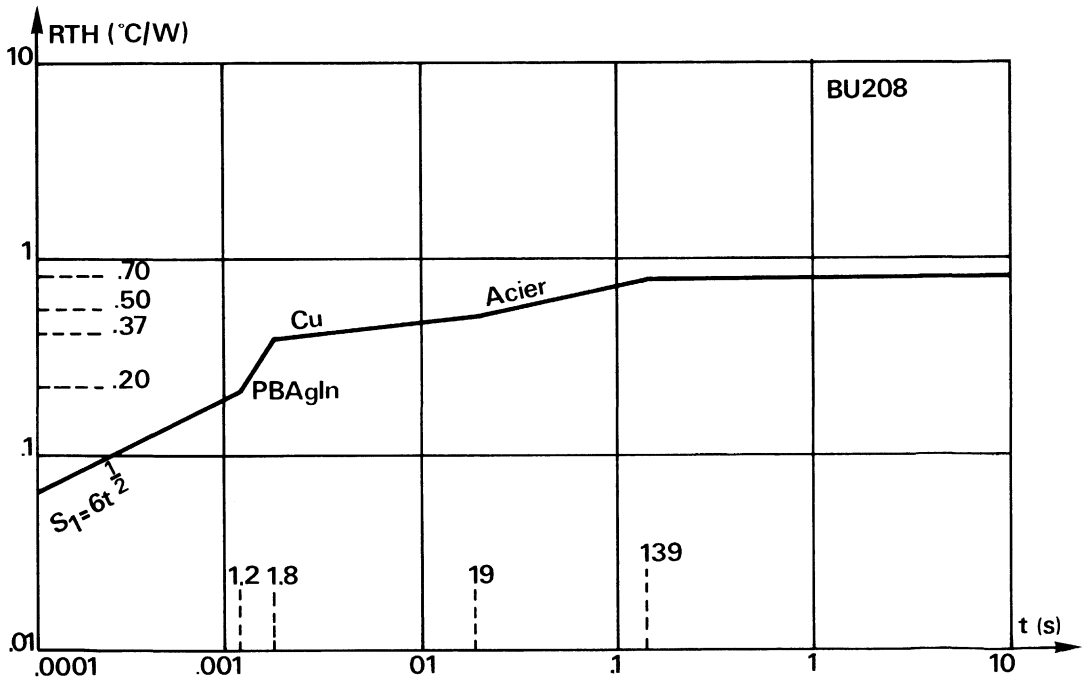


Figure 1-9 – Asymptotic diagram of thermal resistance of BU208

If we now consider the MJ10051 in the high current package (case 346): this device has four parallel chips mounted on a copper heatsink, 1.5 mm thick.

We can take the preceding table, looking at copper, and apply a corrective factor of 4 given that the active surface of an MJ10051 chip is equal to that of a BU208 silicon = .05 and PbAgIn = .10 and the copper = .13.

Transient times are identical to previous ones as they include only the physical parameters of the material and the thickness of the components which are identical. The silicon curve is $\frac{1}{A}\sqrt{\frac{4}{\pi}\frac{1}{.95 .85 \times 2.3}}\, t^{\frac{1}{2}} = 1.45 t^{\frac{1}{2}}$

which is the first section of the complete curve for the MJ10051 as shown below:

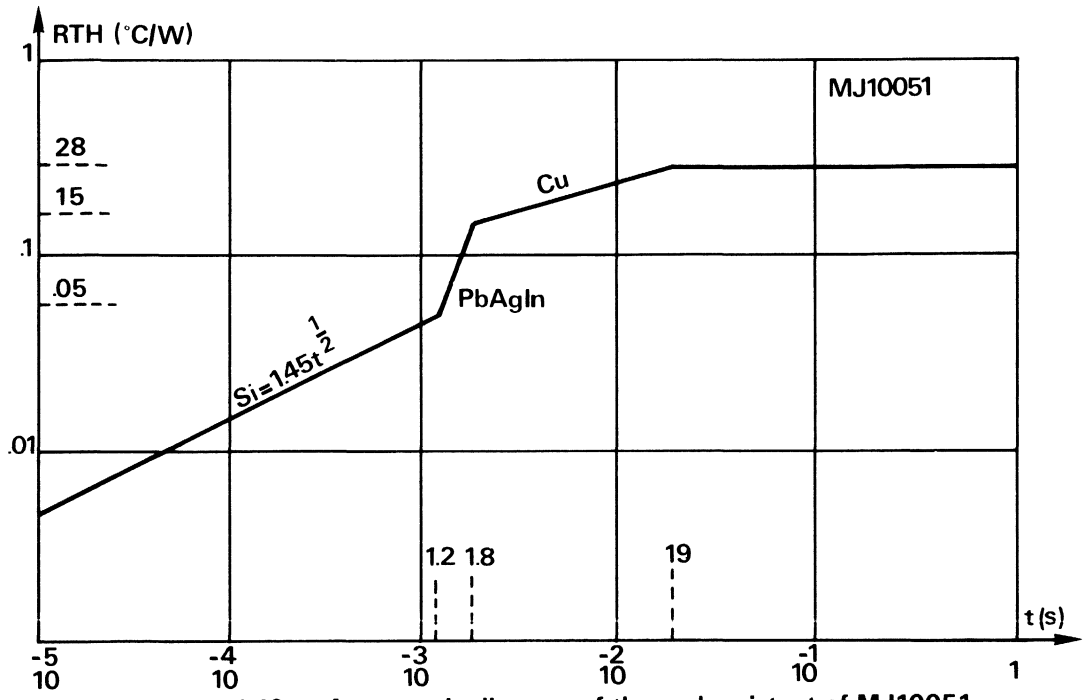


Figure 1-10 — Asymptotic diagram of thermal resistant of MJ10051

A-7. Pulse response of semiconductor components

A-7.1. A SINGLE POWER PULSE

There are many situations where a non-rectangular power pulse may need to be converted to an equivalent rectangular pulse in order to analyze the thermal response.

For waveforms that can be expressed as a simple function such as the sinusoidal and triangular waveforms shown in Figure 1-11. The effective value can be used for the height of the rectangular equivalent. Then by setting the area of the non-rectangular waveform equal to the area of the equivalent rectangular waveform.

The width of the equivalent waveform can be determined as shown below in a) and b).

A-7.1.1. For the sinusoïd, effective value is:

$$Prms = .707\ Ppeak$$

The area under the sinusoïd is $2/\pi = 0.636$, setting this equal to the area under the equivalent rectangular waveform gives $0.636 = (0.7P)t$, and then solving for

$$t_1 = \frac{0,636}{0,707} = 0,91\, t$$

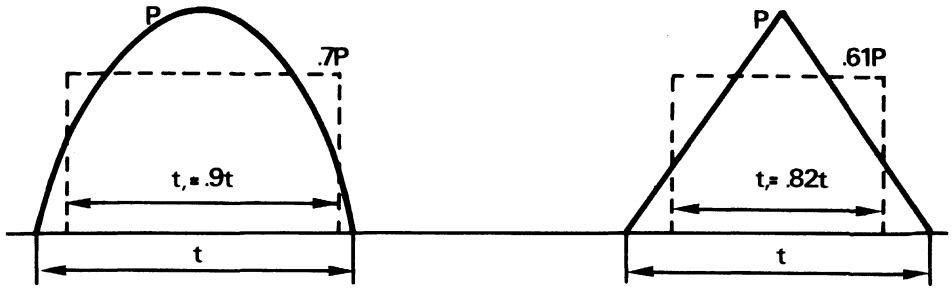
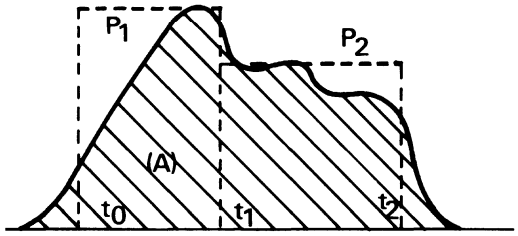


Figure 1-11 – Normalized power pulses

A-7.1.2. For the triangular waveform, a worst case analysis would result by assuming that the triangular waveform can be expressed as a $\sin^2$ function. Since the area under the $\sin^2$ function is 1/2, and the effective value $\sqrt{3/8}$ or~0.61, the eight of the equivalent rectangular waveform would be .61P while the width would be t, $t_1 = \frac{0,50}{0,61} = .82t$

A-7.1.3. For a complex pulse the rectangular equivalent can be approximated. By added a series of smaller rectangular equivalents as shown in Figure 1-12.



$$P_1(t_1-t_0)+P_2(t_2-t_1)=A$$

Figure 1-12 – Model for complex power pulse

With the power pulse converted to an equivalent rectangular pulse the temperature rise can now be calculated from $\Delta T = P$ (transient R).

Transient R for the equivalent rectangular pulse can be found from the curves that were developed in this section (i.e. Figure 1-9). Most manufacturers publish normalized curves as shown in Figure 1-13 which is conjunction with $R\Theta_{JC}$ as follows:

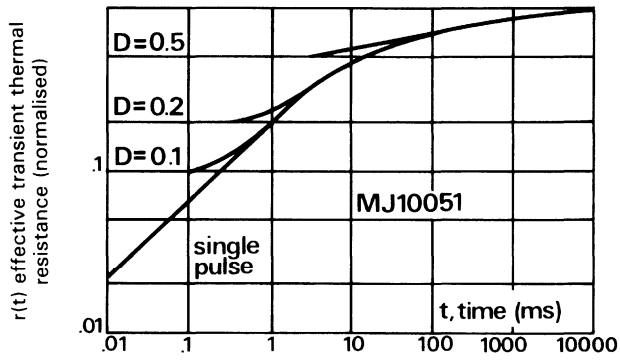


Figure 1-13 – Normalised thermal response of MJ10051

$\Delta T = PR\Theta jc\ r(t)$

For this example, if $P = 25\ A \times 600\ V = 15000\ W$ for 10 microseconds:

Then $\Delta T = 15000 \times 0{,}25 \times 0{,}02 = 75°C$

i.e.: $Tj = \Delta T + TA = 75 + 25 = 100°C$.

It is generally accepted that for pulses significantly below steady state conditions and low duty cycles that the temperature decrease in the same manner in which it increased.

A-7.2. A SERIES OF POWER IMPULSES.

A-7.2.1. Random pulses.For a series of random pulses the **superposition** principle is applied which supposes that the cooling down of a product follows the same laws as its heating, the junction temperature after a series of pulses is the algebraïc sum of preceding heating and cooling cycles (see Figure 1-14).

This method can be applied when the total time of heating is less than the time to reach steady state.

We get: $\Delta T_1 = P_1 r(t1)\ R\Theta jC$

$$\Delta T_3 = \left[P_1 r(t3) - P_1 r(t3-t1) + P_2 r(t3-t2)\right] R\Theta jC \qquad (12)$$

$$\Delta T_5 = \left[P_1 r(t5) - P_1 r(t5-t1) + P_2 r(t5-t2) - P_2 r(t5-t3) + P_3 r(t5-t4)\right] R\Theta jC$$

Generally the last 3 pulses only influence junction temperature at moment t (3rd pulse).

A-7.2.2. **Pulses equal in size and length: uniform pulse series.**

General cases: – at the end of the 1st pulse, as for a single pulse

– at the end of one impulse, in a stabilized state $\Delta T_j = P\,R\Theta c\ r(t_1 D)$

On Figure 1-12, we can read off the desired duty cycle condition, for example $\delta = 0.5$ for $t = 1$ ms gives us $r(t_1\ D) = .5$ and we have $\Delta T_j = .5 \times .25 \times P$ so .125 P

If we assume $Tjmax = 150°C$ and T ambient $= 25°C$, we get $P = 1000$ W i.e. double the nominal power capability of the product, which is normal for pulsed conditions of 50%. We can obviously use the superposition principle but calculations are longer.

Special cases

Using average power to find the temperature at the end of the $n+1$ pulse, we get:

$$\Delta T_{n+1} = \left[\frac{t}{\tau} r(t_{2n-1}) + (1-\frac{t}{\tau}) r(1+\tau) + r(t) - r(\tau)\right] P_D\ R\Theta jC$$

Assuming that $PD = 500$ W, $R\Theta JC = .25$ (MJ10051),Δt = width of pulse = 5 ms, period $\tau = 20$ ms and if we want to find the tenperature at the end of the 5th pulse, we have:

$n+1 = 5$ $\qquad$ $n = 4$ $\qquad$ $2n-1 = 7$

$t2n-1 = t7 = 65$ ms.

On the curve (Figure 1-13) we have: $r(65) = .70$

$r(25) = .6$ $\qquad$ $r(5) = .4$ $\qquad$ $r(20) = .55$

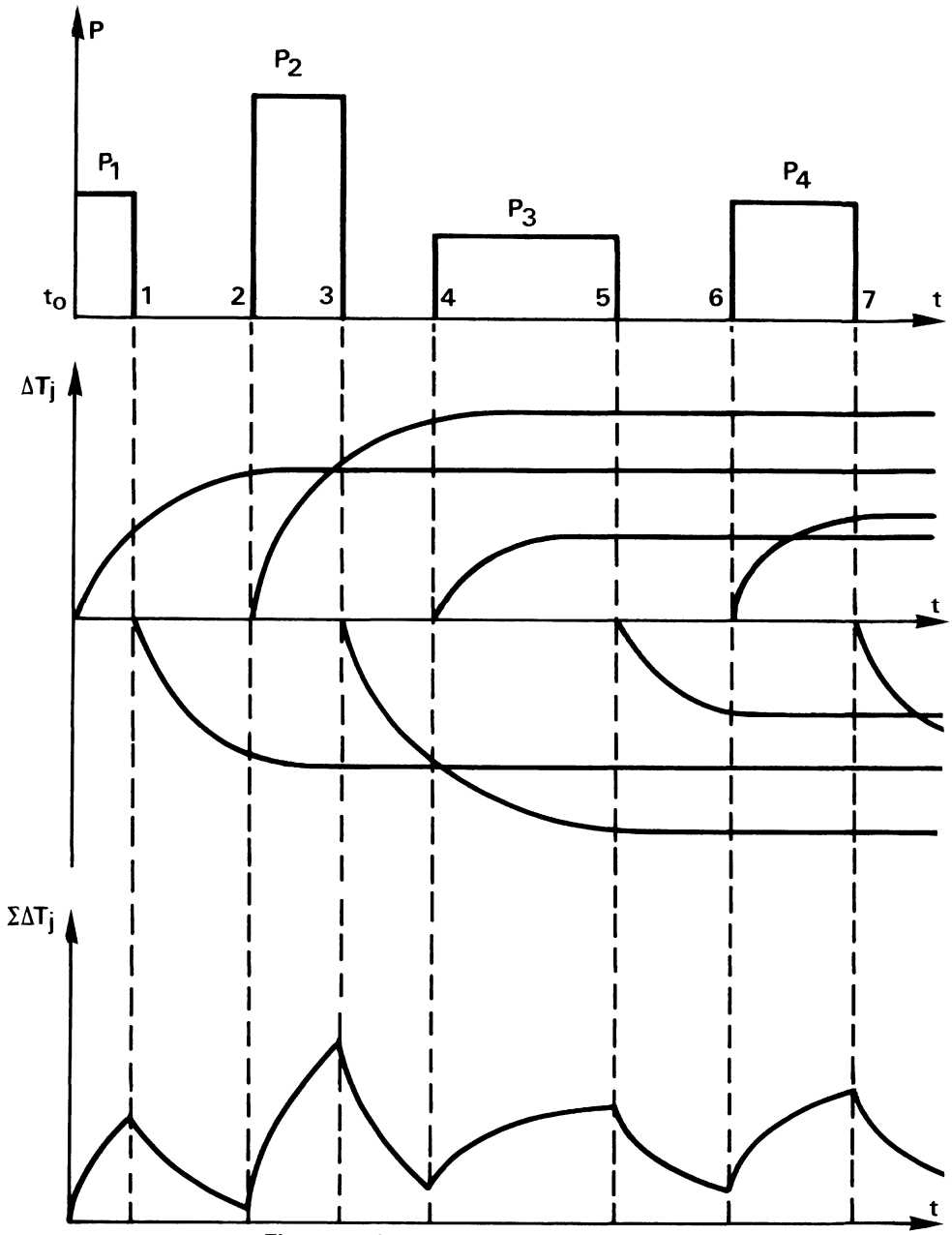


Figure 1-14 – Superposition principle

i.e.:

$$\Delta Tn+1 = \left[\frac{5}{20}\,(0.70)+\left(1-\frac{5}{20}\right)\,0{,}60+0{,}40-0{,}55\right]\;500\times.25$$

$$= 125\;\left[0{,}14+0{,}45+0{,}4-0{,}55\right] = 56°C$$

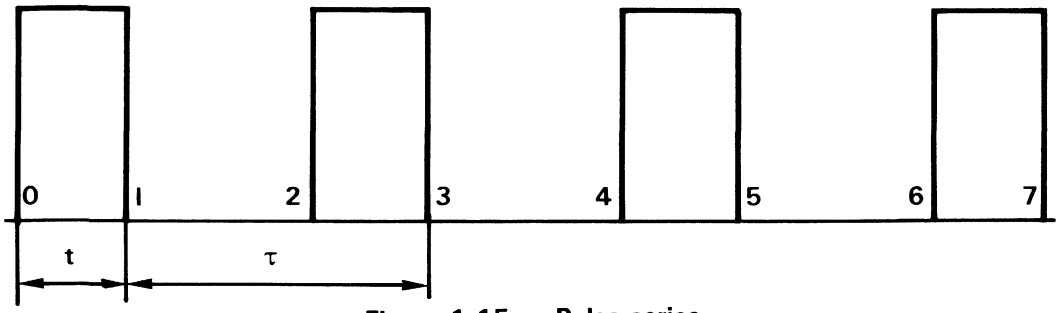


Figure 1-15 – Pulse series

If formula 12 was used we would obtain:

$$\Delta T5 = \left[r(85) - r(80) + r(65) - r(60) + r(45) - r(40) + r(25) - r(20) + r(5) \right] \; 500 \times .25$$

$$125(0{,}00 + 0{,}01 + 0{,}02 + 0{,}04 + 0{,}4) = 0.47 \times 125 = 59\,^{\circ}C$$

Both formula can thus be used.

B) Thermal analysis for long pulses

B-1. Thermal parameters of transistors

B-1.1. THERMAL RESISTANCE OF CHIPS

As we have seen, thermal resistance of the chip in relation to the case is a function of the area of the chip and of the material on which it is mounted, this can then be seen in Figure 1-16 as a function of the die area:

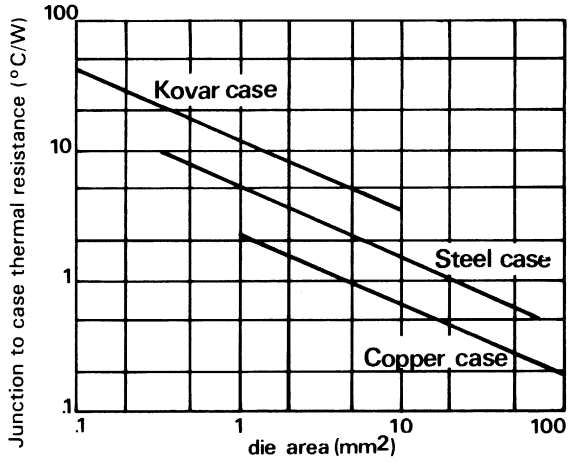


Figure 1-16 – Thermal resistance of chips

B-1.2. THERMAL CAPACITY

The thermal capacities of various cases are given in the table below.

Remember that this was calculated using the formula:

$$C\theta = \text{weight} \times \mathbf{C}$$

Table 1-5

	Aluminium	Steel	Copper	Copper High current package Case 346 Motorola
Weight (g)	7	12	15	50 g copper 50 g epoxy
Thermal capacity $C\theta$:J/°C	6.3	5.4	5.6	20 + 30 = 50

B-2. Application of power

When power is applied, the thermal system operates like the equivalent electrical system (see paragraph B-1.).

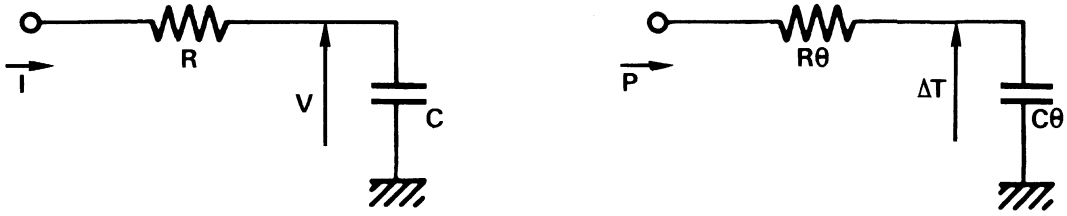


Figure 1-17 – Thermal analogy

Therefore the curves shown in Figure 1-18 can be drawn to simulate the thermal response of the system.

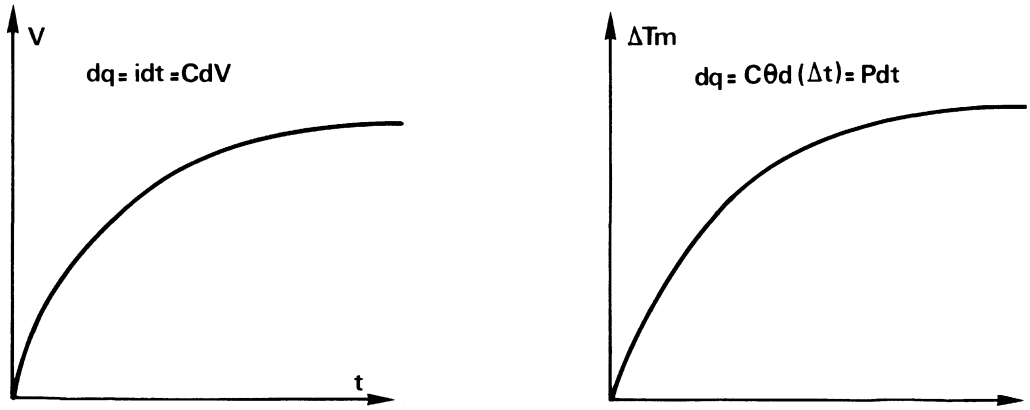


Figure 1-18 – Response to a step function

Example: the thermal capacity of the Motorola high current package from the previous table is = $C\theta = 20 + 30 = 50$ J/°C.

The thermal resistance of the MJ10051 is 0.25°C/W and one time constant for this device on an infinite heatsink can be found from: $\tau = R\theta C\theta = .25 \times 50 = 12.5$ seconds

The curve in Figure 17 has as its equation: $\Delta T = \Delta T_m (1 - \exp \frac{-t}{\tau})$

So, we can say that when we apply a power step to this product, its temperature will rise to 60% of its equilibrium temperature in 12.5 seconds.

If we wished to know the time required to obtain 99.9% of its equilibrium temperature, we would need:

$\frac{\Delta T}{\Delta Tm} = .999 = 1 - \exp\frac{-t}{12.5}$ or $\exp\frac{-t}{12.5} = .001$ or $t = -12.5 \text{ Log } .001$

$t = -29 \quad \text{Log}_{10} .001 = -29(-3) = 87$ seconds

It takes about 87 seconds for this device to reach its thermal equilibrium condition. For cooling we have the same relationship: $\Delta T = Tm\,(e^{-t/\tau})$

If we wanted to know the time required to return to 1% of ambient we calculate as follows: $0{,}01 = (\exp\frac{-t}{12.5})$ $t = -29 \text{ Log } 0.01 = 58$ seconds

B-3. The radiator in ambient air

Dispersion of calories can be done in 3 different ways:

- conduction (already seen) $R\Theta = e/k$
- radiation and
- convection

B-3.1. RADIATION

The rate of calory-transfer by given area can be found using the STEPHAN-BOLTZMANN law (13) $HR = 6.10^{-12}\ E\ (TB^4 - TA^4)$ in $W/cm^2.{}^\circ C$ (13)

TB and TA = temperature of radiant surface and ambient in °C.

E being emissivity (see following Table 1-6).

Table 1-6

Material	E
Anodized aluminium	0,7 – 0,9
Polished aluminium	0,05
Polished copper	0,07
Oxidized copper	0,7
Oxidized steel	0,7
Oil paint (any color, varnish)	0,9
Alumine (white)	0,9

For example: a TO3 of E = 0.9 and TB = 100°C TA = 40°C

$HR \cong 610^{-4}$ W/cm²°C

B-3.2. FREE CONVECTION

The following equation gives us the transfer coefficient in calm air at sea level up to a temperature of 800°C: $H_C = 4.10^{-4}\,(\frac{\Delta T}{L})^{\frac{1}{4}}$ in $W/cm^2.{}^\circ C$ (14)

L being the length of the vertical part of radiator, ΔT the difference of temperature between the surface and ambient air.

For example, a vertical TO3 (L = 2.5 cm) of temperature = 100°C, in calm air at 40°C, gives us: $H_C = 10^{-3}$ $W/cm^2.{}^\circ C$

B-3.3. FORCED CONVECTION

The general formula is written as: $H = 2.10^{-2}\sqrt{\frac{v}{L}}$ with v = airspeed in m/seconds, L in cm

The thermal resistance convection curve verses air speed is shown in Figure 1-19.

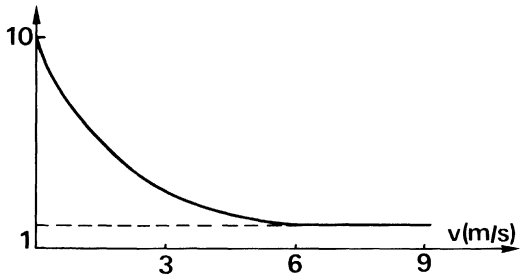


Figure 1-19 - Thermal resistance versus air speed

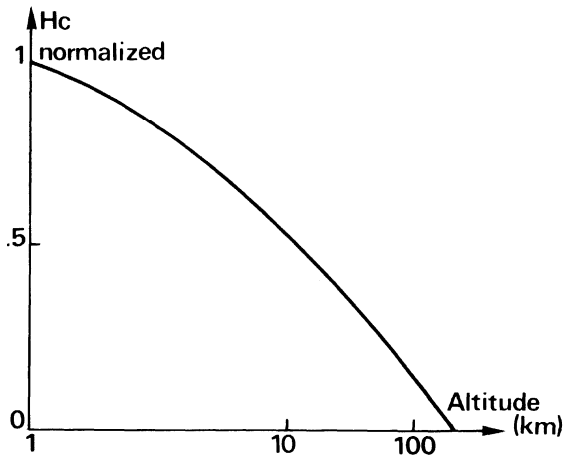


Figure 1-20 - Convection coefficient versus altitude

From this curve, we can see that air moving at 6 m/s is sufficient to reduce thermal resistance by a ratio of about 10 to 1.

We can consider then, that convection plays and important part in heat transfer.

In free air heat is transfered at 70% by convection and 30% by radiation, as soon as ventilation is included, the radiation part drops to about 2% the total. A since convection is a more efficient means of heat transfer, the temperature of the device being cooled decreased significantly. Figure 1-20 shows the relationship between convection heat transfer and altitude, another factor that may need to be considered when analyizing a thermal system.

B-4. Continuous use

The thermal resistance of a TO3 can be calculated in free air as follows:

$R_{CA} = \frac{1}{(HC+HR) \times \text{area} \times 2 \text{ sides}} = \frac{1}{10^{-3} \times 6 \times 2} = 40$ °C/W Its thermal capacity being 6J/°C (from II-A-2), we get $R\Theta C = 240$. The formula for its thermal resistance is

$$R\theta JA = 40\,(1-\exp\frac{-t}{240})$$

Example = assume a 180 W pulse is applied for 1 second to a TO3 device, what is its temperature rise at the end of 1 second? $\Delta T = \frac{P}{C\theta} = \frac{180}{6} = 30$ °C

If we want the time required for the case to return to ambient temperature + 1 °C when the power pulse is removed we have: $\Delta T = \Delta T m \exp\frac{-t}{240} = 30 \exp\frac{-t}{240} = 1$

or t = 240 Ln 30 or 550 log 30 = 550 × 1,477 = 820 seconds.

An identical calculations for the high current case (C346) MJ10051 is as follows:

$$RC\theta = \frac{10^3}{3 \times 25 \times 2} = 6 \text{ °C/W in free air}$$

the thermal capacity of this case is $C\theta = 50J/°C$ (Paragraph II-A-2) therefore $R\theta\ C\theta = 6 \times 50 = 300$ seconds resulting in the general equation $R\theta jA = 6\,(1-\exp\frac{-t}{300})$

2. Safe operating areas

A) Forward bias safe operating area (SOA or FBSOA)

A-1. Introduction

This area is limited, in general, by 4 straight segments on logI × logV graph (see Figure 1-21).

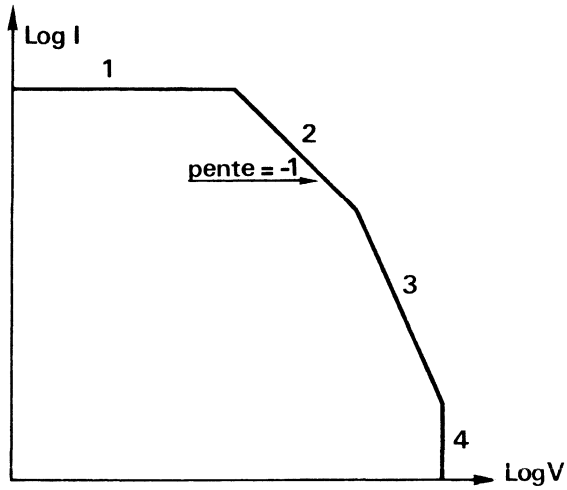


Figure 1-21 – Typical FBSOA

A-2. The first straight segment (1), parallel to the voltage axis, gives us a continuous current limit, typically this limit is based on limiting the current density in the bonding wires to a specific level. However in some cases the device chip size may be the limiting factor. The military specification MIL38510 specifies the maximum current density for bonding wires with the following relationship. $I = Kd^{3/2}$ (1) Where d is equal to the wire diameter in millimeters.

K depends on the type and length of the wires. Values for various materials are shown in Table 1-7.

Table 1-7

	L<1mm K	L>1mm K
Aluminium	171	118
Gold	234	160
Copper	234	160
Silver	117	82
Others	70	48

The information in Table 1, and equation (1) can be used to determine that an aluminium wire of 10 mils in diameter (0.25 mm) and a length of over 1 millimeter would take a continuous maximum current of: $I = 118 \times 0{,}25^{3/2} \simeq 15A$

A-3. The second segment (2) on the SOA curve is the D.C. Power dissipation limit. $P = VI = \text{constant}$, represents this segment on the SOA curve.
This maximum power is limited to a level which will satisfy this relationship:
$T_{j_{max}} = P.R\theta_{j-c}$

Tjmax is the rated junction temperature defined for reliable operation. $R\theta$ jc being junction-case thermal resistance which is a function of chip size and case materials. For this portion of the SOA curve the temperature gradient is homogeneous across the entire chip. At higher voltages the electric field can produce a non-homogeneous temperature gradient and effectively reduce the power handling capability of the device. This situation exists for segments 3 and 4 and will be discussed next.

A-4. An analysis of segment 4 will help to explain segment 3. Therefore segment 4 will be looked at first.

A-4.1. Two breakdown phenomena can expect for segment 4.

A-4.1.1. In the presence of a strong electric field, the carriers may have enough energy from the network atoms to free other carriers, these, in turn generate other electron – hole pairs and we get a multiplying phenomenon right up until the device avalanches. This phenomenon is reversible. The field limit Ecr is a function of the doping of the lightly doped collector zone (Figure 1-22).

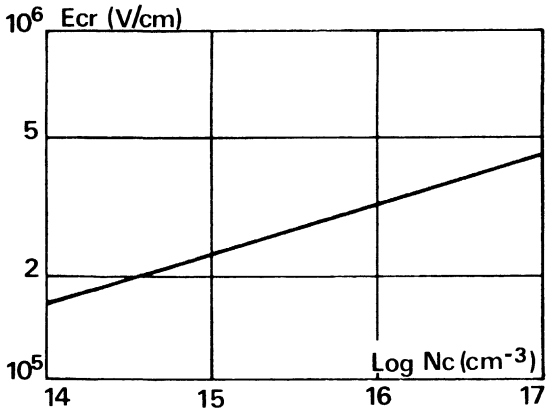


Figure 1-22

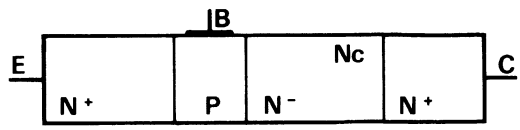
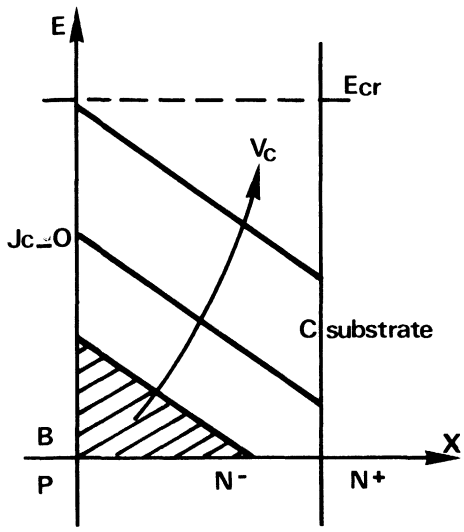


Figure 1-23

Figure 1-22 — Field limit Ecr versus collector doping density.

Figure 1-23 — Represents an NPN high voltage power transistor.



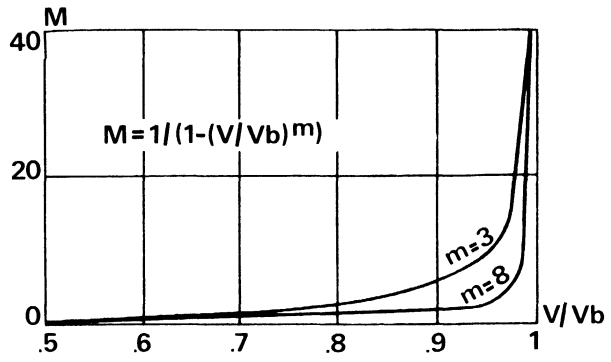


Figure 1-24 — Electric field at BC junction

Figure 1-25 — Miller factor versus V/Vb

Which develops in the lightly doped region of the collector, Figure 1-24, also represents

Poisson's equation: $\frac{dE}{dx} = \frac{1}{\varepsilon}\left(qNc - \frac{Jc}{v}\right)$ (2)

v = being the speed of the carriers ($v = \mu_0 \epsilon$)
Jc = the current density
μ = carrier mobility
ϵ = electric field

If we consider the phenomenon at low currents, we can say $\frac{dE}{dx} = \frac{1}{\varepsilon} q\ Nc$

Since Nc is practically constant for an epitaxial transistor dE/dx is constant as indicated in Figure 1-24. The voltage supply is proportional to the area under the straight line dE/dx.

If we increase the supply, the dE/dx line will rise up to the Ecr field limit and create an avalanche or first breakdown.

The multiplying avalanche factor has been stated by Miller in the following formula:

$$M = \frac{1}{1-\left(\frac{V}{VB}\right)^m}$$

V = voltage supply
V_B = avalanche voltage
m = multiplying factor depending on material

Table 1-7

Semiconductors	N Type	P Type
Silicon	4	2
Germanium	3	6

The M variations with V/VB, m are shown in Figure 1-25.

The value of VB depends on the material and technology of the junction.

For an abrupt junction, Figure 1-26 applies.

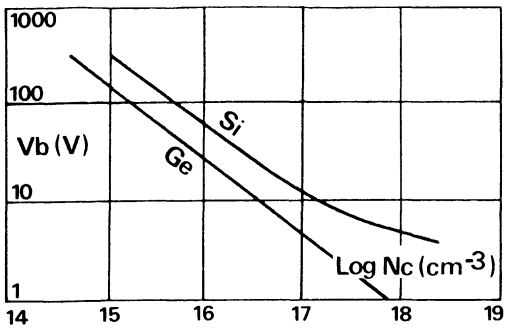


Figure 1-26 — Avalanche voltage versus material

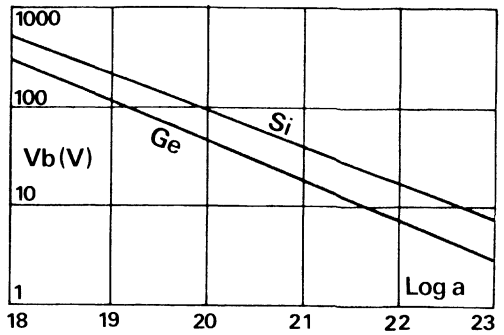


Figure 1-27 — Diffusion curve slope

For graduated junctions (triple diffused technology), Figure 1-27 applies.

The general equation for total transistors collector current is: $I_C = M(\alpha I_E + I_{CB})$

ICB being the reverse diffusion current in volume or charge regenerator.

If we write $IE = IC + IB$ we have: $Ic = \frac{M}{1-\alpha M}(ICB + \alpha IB)$

For the avalanche $\alpha M > 1$, the base current reverses itself and becomes IBR, giving:

$$Ic = \frac{ICB - \alpha IBR}{1-\alpha(VCE/Vs)^m} \quad \text{or again} \quad VCE = VB \left\{1-\alpha+\alpha\left[\frac{IBR}{IC} - \frac{ICB}{IC}\right]\right\}^{1/m} \tag{4}$$

This equation does not take into account the possible reverse current from the emitter. When IC increases compared to IBR, we can write:

$$VCE + VB\,(1-\alpha)^{1/m} \text{ setting } VCE = V\alpha M \text{ gives } V\alpha M = VB\,(\beta+1)^{1/m} \tag{5}$$

which is graphically represented in Figure 1-28.

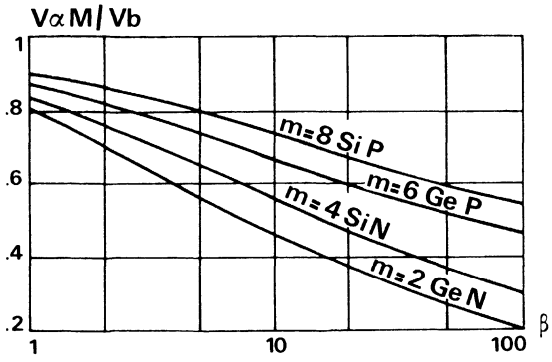


Figure 1-28 — Avalanche breakdown versus gain

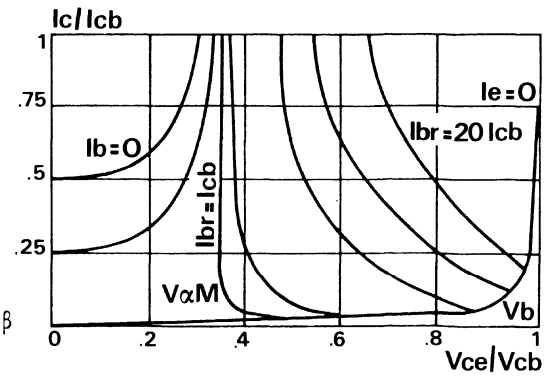


Figure 1-29 — Avalanche characteristics

The reference material is the lightly doped region of the collector (N-) or drift zone.
A graphic representation of the avalanche characteristics are shown in Figure 1-29.
If the actual depth of the N- region is made small, the breakdown voltage decreases proportionally from the following relationship:

$BVCBO = \frac{We}{xmB}\left(2 - \frac{We}{xmB}\right)VB$ xmb being the minimum depth of the N- region to sustain VB. We: being the actual N- region depth.
Figure 1-30: Is a graphical representation of this relationship.

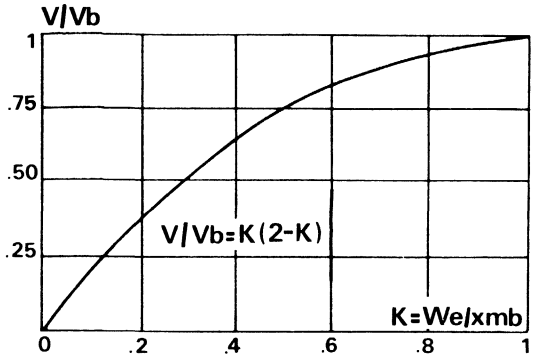


Figure 1-30 — Breakdown voltage versus collector depth

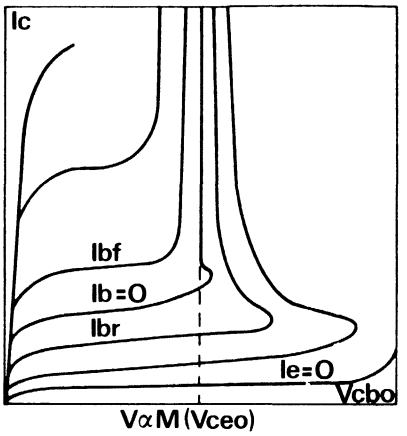


Figure 1-31 — Avalanche breakdown curves

A-4.1.2. If N-region is sufficiently spread and the base region is highly resistive with its Wb thickness thin emitter collector punch trough Vpt occurs when the electric field sufficiently affects the emitter base function prior to avalanche.
At this moment the breakdown voltage of the transistor is limited by Vpt instead of VB.

A-4.2. For the standard emitter configuration we can say that BVCES = BVCBO.
If the device is limited by the avalanche then BVCES = BVCBO − BVEBO, if punch through is the limiting factor then:
BVCES = BVCBO − BVEBO = VpT. For the BVCEO we have:

$$BVCEO = V\alpha M = \sqrt[n]{\beta} \qquad (7)$$

if the device is not limited by VpT, the curves shown in Figure 1-31, apply.

A-4.3. TECHNOLOGICAL COMPROMISES

We know that VCEOsus = K2 Wc
Wc = being the metallurgical depth of the collector. K2 being equal to ≈ 10V/μm for an NPN transistor.

We also have:
$G = HFE\ IC = K1\ AE/Wc^2$ AE being the emitter area ie $G = \frac{K3}{(VCEO\,sus)^2}$ An more precise analysis gives us: $G = \frac{K3}{(VCE\,sus)^{2.3}}$

which is very restricting, because in order to increase VCEOsus significantly while maintaining high current gain requires a substantial increase in chip area.

A-4.4. TEMPERATURE VARIATION

The breakdown voltage of a planar junction increases with temperature because the level of recombination increases as the square of IL, at the same time the level of generation increases linearly with tenperature and the electric field increases, thereby restricting the number of collision.

A-5. Second breakdown – 2nd BV under forward biased conditions

Physical phenomenon: if a power transistor is driven into avalanche (ib = 0) and allower, to reach Im current, a sudden collapse of voltages will be observered and the current through the transistor will be limited only the external circuit. This phenomenon is called, second breackdown and is represented graphically in Figure 1-32.

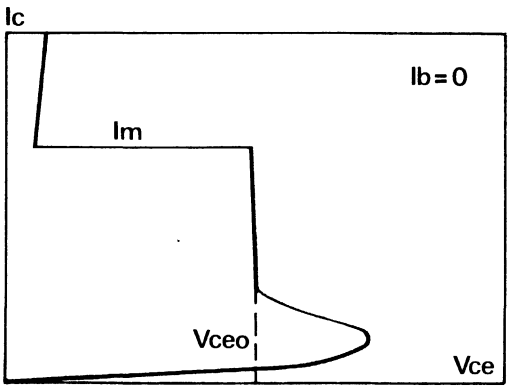


Figure 1-32 – Second Breakdown

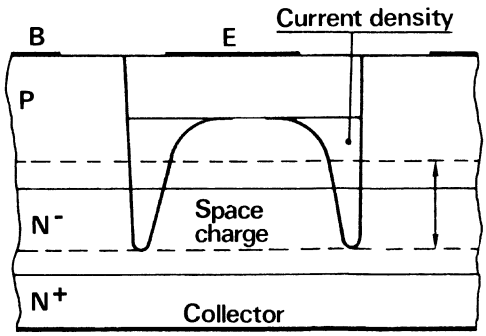


Figure 1-33 – Current density under the emitter finger

This phenomenon was first described in 1958. Later it was discovered that it was not necessary to pass through the first avalanche to have a second breakdown and that it could come about through forward biasing of the base.

The Im current decreases as collector voltage increases by observing this phenomenon with short power pulses it can be seen that the material is temperature depend.

The Im × Vce product is always less than the Pmax of the device. This phenomenon is a basic property of semiconductors. In 1966, using an N+N N+ structure (i.e. a slice of so-called intrinsic silicon between 2 slightly resistive ohmic contacts), Japanese researchers caused the same phenomenon to appear when a critical voltage current point was reached.

The temperature of the crystal at this moment was between 200 and 300°C inclusive for the resistivities of the materials used (temperature inversely proportionate to resistivity). This temperature corrresponded with that of the intrinsic conduction of the semiconductor (that is to say, at the moment when it becomes identical to a conductor). It was also noted that the phenomenon of intrinsic conduction does not immediately distroy the materials.

Today, we know that at least two phenomena are responsible for the second breakdown in power transistors.

A-5.1. A THERMAL PHENOMENON

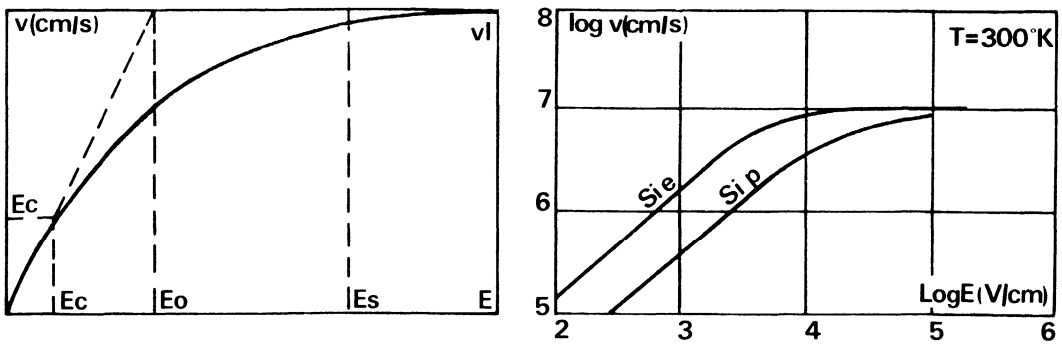
When a transistor is forward biased, a transverse electric field appears in its active base region, because of bulk resistance, this field tends to grownd current towards the edges of the emitter fingers: Figure 1-33.

Since the current density increases significantly at the edges of the emitter fingers overheating may occur locally with the appearance of ''hot spots''. These in turn created low resistive paths for the current and the current density to increase further resulting in thermal instability as studied by Scarlett and Schokley in 1963.

Depending on the voltage and current levels, this phenomenon can be degenerative to the point of the 2nd BV and the destruction of the transistor by punch through on the edges of the emitter fingers.

But it can also be relatively stable and not reached second BV, this will appear as instability of the breakdown waveform on a scope or curve tracer.

We said previously that carrier speed is $v = \mu o\, \epsilon$ this is only true in reality for weak electric fields, when the electric field is increased A value of ϵ_C fields is reached, after which, speed does not increase and: $v = \mu o \sqrt{\epsilon \epsilon_C}$ continued increase in field strength will produce a saturation point, ϵ_S, at this point the speed is constant which gives: $v = \mu o \sqrt{\epsilon_C \epsilon_S}$ This relationship is shown graphically in Figure 1-34.



Speed versus electric field **Figure 1-34** **Speed versus materials**

If we again look at the high voltage power transistor in Figure 1-23, and the $\epsilon = F(x)$ relationship we get the following Figure 1-35.

For a constant VCB voltage(area below the curve is constant) and an electric field less than Es, the current is small at first, the field slope as a function of x is identical to Figure 1-24.

When the current is increased, Jc increases, electron speed must increase and for this to happen, the field must increase. This can only be done by displacing the curve as shown in Figure 1-35. Since a function can be characterised by the fact that dE/dx is infinite, we see that a displacement of the metallurgic collector base junction in the low doped zone of the collector, effectively widens the base (Kirk effect 1962). A limit is reached when the field is at saturation Es, additionaly $Jc/V = qNc$ and $dE/dx = 0$ (flat curve). At this point carrier speed cannot increase, which means that excess carriers must be injected into the N- region. These injected carriers are supplied by the emitter, giving a negative value for dE/dx and a linear relationship of $E = kx$.

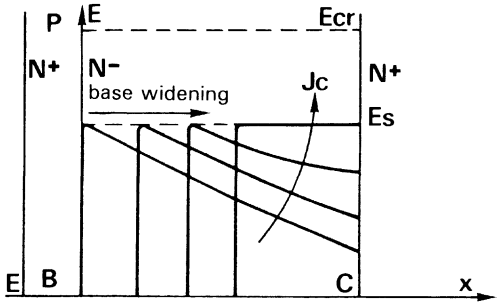


Figure 1-35 — Field versus distance

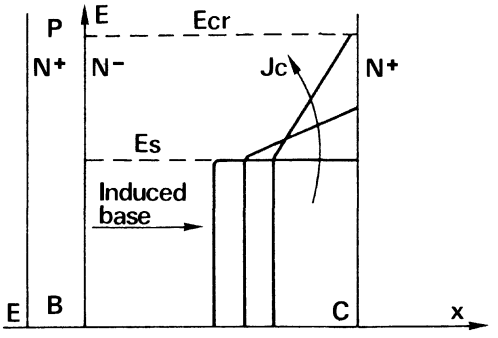


Figure 1-36 — Base widening

For each increase in I there is an increase in Jc this widening of the base and steepening of the slope continues until the field at interface N− N+ reaches the critical field value Ec, Figure 1-36.

At this moment, the avalanche occurs, a large quantity of electron hole pairs are created, electrons move toward the collector (NPN) and the holes, toward the base: there is an injection of holes due to the avalanche thus the term avalanche injection and the possibility of negative resistance and destruction.

The important phenomenon here is the effect of base widening, resulting in a decrease in transistor gain. If the base current is constant, the local current density decreases and hot spots are reduced, resulting in a stabilisation effect. This effect could not exist in single diffusion transistors.

P.L. Hower, in 1973 gave a formula for stability factor S: $S = RTH\ VCE\ \delta Ic/\delta T$ (8)

If $S < 1$, the inhomogeneities of junction temperature decrease with overall temperature and the product becomes stable.

If $S > 1$, as soon as a hot spot appears, the system tends to degenerate with time (1 ms and over).

Suppose that the 2nd BV survives when $S = 1$, the power dissipation in the device is:

$$P_{SB} = Ic\ Vce = \frac{1}{RTH}\ \frac{Ic}{\delta_{Ic}/\delta_T} \qquad (9)$$

We see immediately that if we want to increase PSB, we must decrease RTH i.e. increase the size of the chips assuming that current density stay constant.

We can predict the stability point by the formula:

$$Vce\ INTH = \frac{Ic\ Re + Tc\ .\ k/q\ .\ Ln(I1/IC)}{k/q(Ln\ I1/IC-1)\cdot Ic\ R\theta jC} - \frac{Tc}{Ic\ R\theta jC} \qquad (10)$$

Vce INTH: collector – emitter voltage at a given Ic for which thermal stability exists.
Ic = collector current
RE = emitter series resistance
Tc = case temperature (°K)
It is defined by the following equation: $I1 = Ic \exp \frac{-q(VBEJ-Eg)}{KTj} = \frac{qAE\ nio^2}{QB/DB}$ (11)
VEBj = internal base emitter voltage
E_g = forbiden band (S_I = 1.1eV)
Tj = junction temperature (°K)
AE = emitter area
Nio = 2.46 10^{19} cm^{-3} for the silicon
QB = the number of majority carriers in the base per unit of area
DB = the coefficient of diffusion of minority carriers in the base
QB/DB = is often called GUMMEL number
All these physical values can be measured or calculated.
RE (emitter resistance) can be measured on a curve tracer connecting the base to the collector terminal, emitter to ground and leaving the collector open.

The waveform on the curve tracer is shown in Figure 1-37.

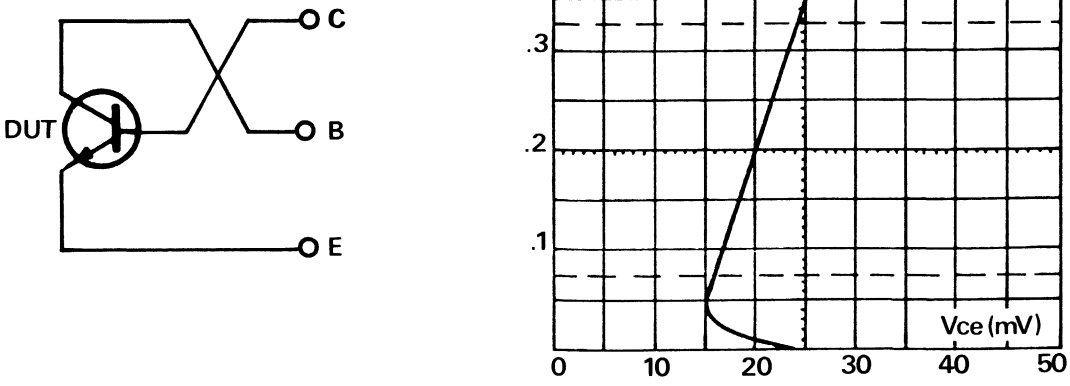


Figure 1-37 – Emitter resistance measurement

The value of RE is the slope (VE/IE) of this curve at the higher current levels.
For this example RE = 33 mΩ to calculate I1, we can also use a curve tracer to find VBEJ. For this measurement the device is mounted normally in the test jig, the measurement is taken at low IE, so that results are not distorted by the presence of RE, and assume IE = Ic on the horizontal axis set value of VBE on the screen (Figure 1-38).

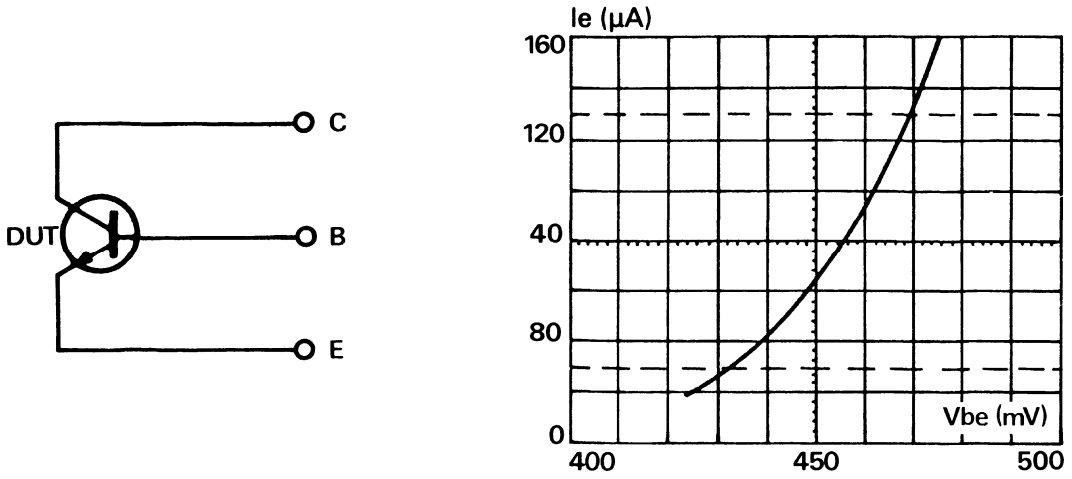


Figure 1-38 – V_{BEJ} measurement

For this example IE = 100μA, VBEJ = 460mV and we calculate I1 =

$$10^{-4} \exp \frac{-1{,}6\ 10^{-19}(.46-1{,}1)}{1{,}38\ 10^{-23}\ 300} \qquad 10^{-4} \exp \frac{10250}{414} = 10^{-4} \exp 24{,}8 = 10^{-4}\, 10^{10{,}7} = 10^{6{,}7} = 510^{6}\text{A}.$$

If we wish to calculate Vce INTH for IC = 0.5 and RθJC = 1°C/W, we have: Vce INTH =

$$\frac{0.5 \times 3 \times 10^{-2} + 300 \times 863\ 10^{-7}\ \text{Ln}\ 10^{7}}{863\ 10^{-7}(\text{Ln}\,10^{7}-1) \times 0.5 \times 1} - \frac{300}{0{,}5} = 40\text{V} \quad \text{so Vce INTH} = 80\text{V if RθJC} = 0{,}8\ ^{\circ}\text{C/W}$$

In actual use of power transistors it is not advisable to enter this region, even if there is no degenerative phenomenon.

In fact, prolonged use with hot spots at a temperatures of 200 to 300°C automatically causes parasitic diffusion or long term dislocation, resulting in a significant reduction in reliability.

A-5.1.1. How to detect the development of hot spots?

It is well known that VBE voltage in silicon transistor decreases at about 2 mV/°C.

When hot spots develope the temperature increases suddently and so VBE decreases suddenly.

By observing the changes in VBE as the load (VCE × IC) increases, one can detect the appearance of hot spots (Figure 1-39).

A-5.1.2. What are the technological changes that can be made to the power transistor to improve its performance at second breakdown?

If we take stability factor S (equation 8), we can rewrite it as follows:

$$S = \frac{(T-TA)}{T} \cdot \frac{(kT/q\ \text{Ln}\,(I1/Ic) + (IcRB/HFE)\ \Delta E/kT}{kT/q + Ic\,(RE + RB/HFE)} \qquad (12)$$

assuming the device is controlled by a voltage source. ΔE "activation energy" is approximately 0.15 eV for a triple diffused transistor, 0.05 eV for a planar, and 0.1 eV for a double diffused, kT/q = 26 mV to 300°K.

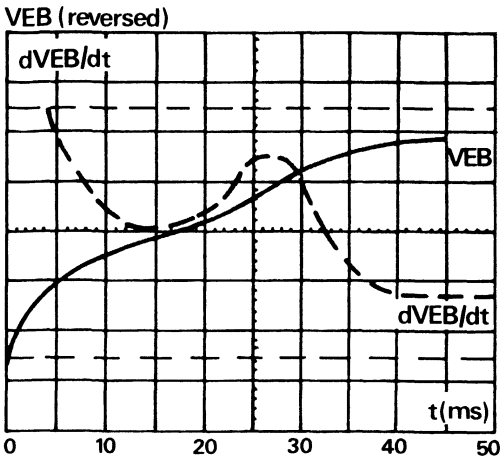


Figure 1-39 — V_{EB} versus time

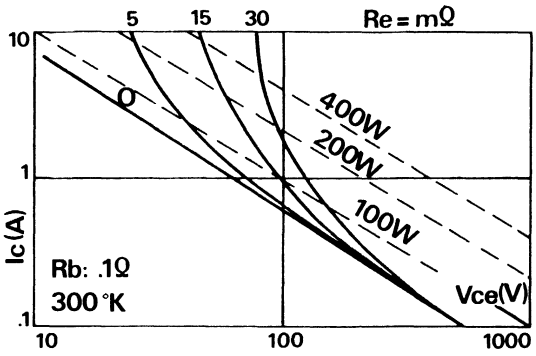


Figure 1-40 — Power dissipation versus emitter resistance

According to formula 12, we see that if we increase internal RE resistance, the stability factor S decreases, if we set S = 1: limit for thermal stability, the level of 2nd BV (PSB – ESB) increases linearly with RE if Ic is held constant. If VCE is held constant, we can say that PSB rises exponentially with RE (Figure 1-40).

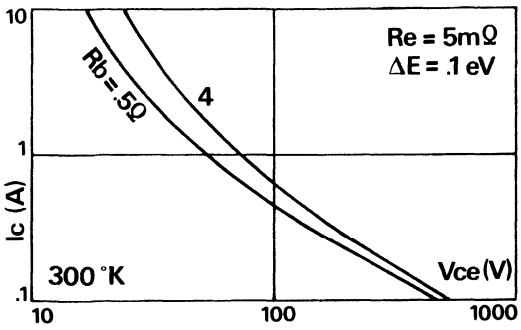
These RE effect only occur at high currents. We say, from equation 9, that we can improve PSB reducing RTH.

Since S is dependent on RE it is also dependent on RB, however its effects are less because of the HFE of the transistor, but are dependent of the variations of HFE verses temperature.

If the HFE increases with temperature, RB contributions is reduced.

If the HFE is independent of temperature, we increase the contribution due to RB.

We can say that, appart from the fact that HFE = f(Ic) in the region where Ic is decreasing: $HFE(T) = \text{constant} \cdot \exp(-\Delta E/kT)$ thus the fechnologies which tend to increase ΔE are more sensitive to the presence of RB. (See as an example the following 2 graphs 1-41 and 1-42):



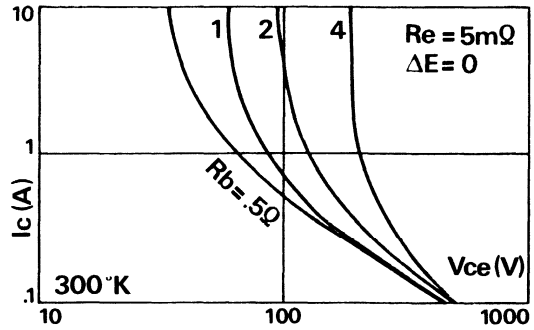


Figure 1-41 and 1-42 — Power dissipation versus base resistance

In spite of its reduced affects, RB has the advantage of not affecting the VCEsat and therefore losses, nor the gain, nor the switching times.

A-5.2. THE AVALANCHE INJECTION

This model is appropriate when high current densities and strong electric fields are simultaneously present in the low-dope N- region of the collector of a high voltage power transistor.

At high supply voltage, the depletion region is very large and the concentration of current is considerable. This means that even if the value is low, current density on the edge of the emitter finger can be very large (see Figure 1-33).

If we take the model of Figure 22 again, and graph $\epsilon = f(x)$ with high VCE = constant we obtain Figure 1-43.

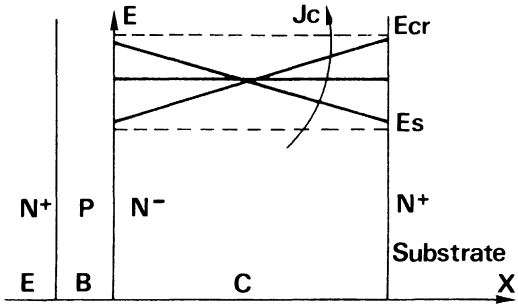


Figure 1-43 — Collector field

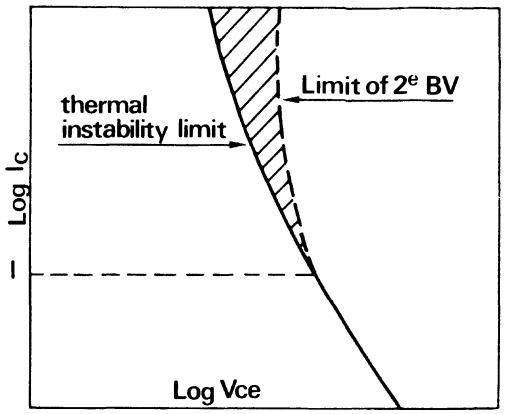


Figure 1-44 — 2nd BV limits

Given a high voltage, leads us to assume that speed is at saturation level, and Poissons's equation applies: $\frac{d\varepsilon}{dx} = \frac{1}{\varepsilon}\left(qNc - \frac{Jc}{v}\right)$

We can simplify the solution by the looking at what hapens when Ic is increased, Jc is increased by electrons injected from the emitter, $v = v_S$ is constant, and there is a decrease of $d\epsilon/dx$ as Jc increases up to $d\epsilon/dx = 0$ (horizontal line) when $Jc/v = qNc$.

The maximum field moves away from the critical Ecr field, the breakdown can now take place at higher voltage.

When $Jc = qv\,Nc$ is passed, the excess electrons compensate the space charge in the depleted N- region and force the curve to reverse.

It becomes negative until the critical field is attained at the interface N – N + + and we get breakdown injection: see thermal phenomenon at the limit of the second breakdown, previous paragraph.

Here there is little or no base widening effect, so there are no stable hot spots in the thermal instability region and we immediately move into the secondary BV (see curve 1-44, below value I*).

The secondary breakdown limit is found approximately on a hyperbole represented by:

$$ISB = \frac{k}{VCE^n} \qquad (13)$$

n being between 1.5 and 4 depending on the types of transistor and junction (gradual or abrupt).

This is always less than the maximum thermal limit given by the manufacturers because in this region only 8 to 10% of the silicon is used for conduction.

Moreover, the stability factor in this region is S = 1 and gives us a mean junction to case temperature as follows:

$\Delta T_{jb} = \frac{TA}{Ln(I1/IC)-1}$ (14) If we take I1 found previously on page 1-28, $I1 = 510^6 A$

$TA = 300°K$ for $IC = 100$ mA, we get: $\Delta T_{jb} = \frac{300}{Ln(510^7)-1} = 18°C$

Because of the logarithmic form of formula 14, one could say that the difference of junction to case temperature in second breakdown state is relatively constant, between 16 and 18°C, which is substantially different than the temperature differences given by manufacturers.

We now have the family of curves I_C vs Vce for a power transistor: Figure 1-45.

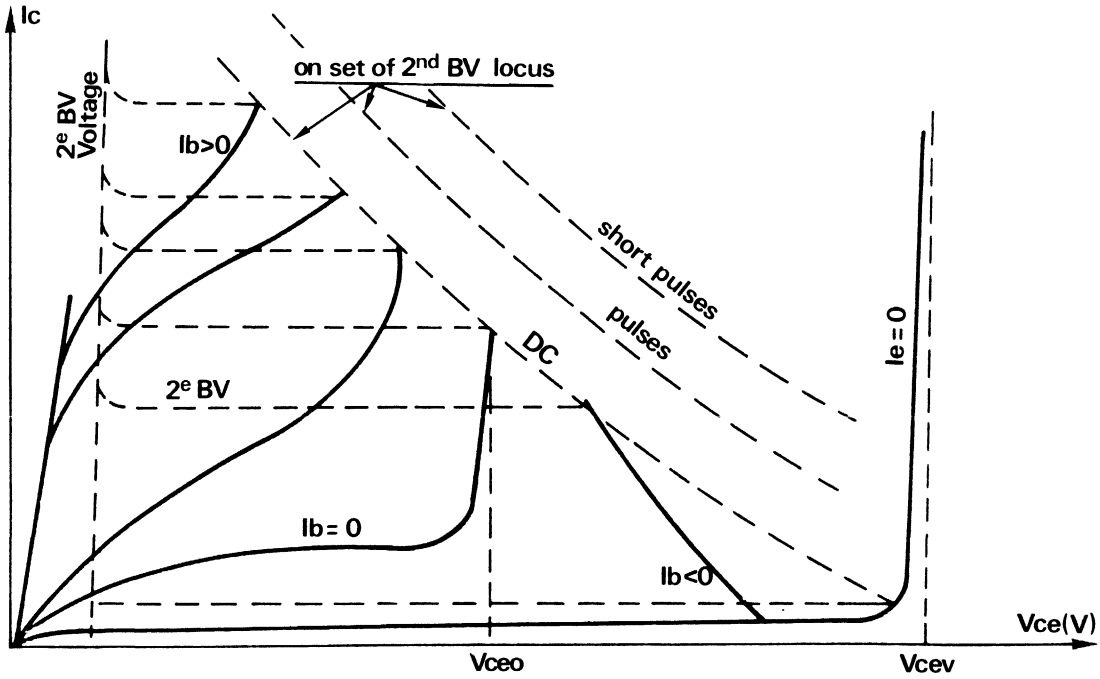


Figure 1-45 — Ic versus Vce

A-6. Thermal resistance at high voltages

The previous paragraph leads us to consider that a products thermal resistance is much higher than indicated by the manufacturers when device is subjected to high voltages.

This phenomenon can be proven by appling the same power pulse to a device but at different potentials, and measuring the junctions temperature by on of two different methods:

- variation of VBE = F(T)
- with infrared radiometer

We have already seen in the "thermal resistance" section, that for short times, the unidimentional heat flow may be used according to the following relationship:

$T(t) - T(0) = K\sqrt{t}$ (15) which is represented graphically in Figure 1-46.

The infrared (IR) measurements have also been marked on this curve.

Two statements can be derived from this:

– when voltage increases, junction temperature increases significantly (VCE 2 = 2.5 VCE 1).

– The conventional measurements reduces the junction temperature even more as the voltage rises because this measurements tends to spread out the temperature (medium temperature) error of – 4 °C at VCE = 40 V, error of – 50 °C at VCE = 100 V.

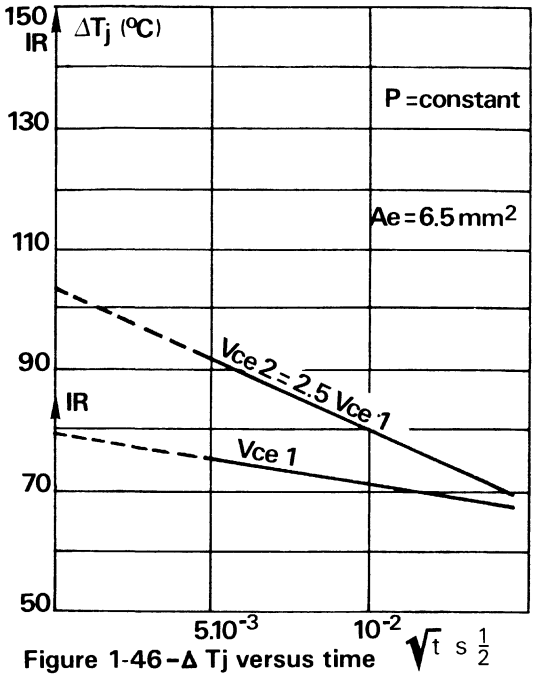


Figure 1-46 – Δ Tj versus time

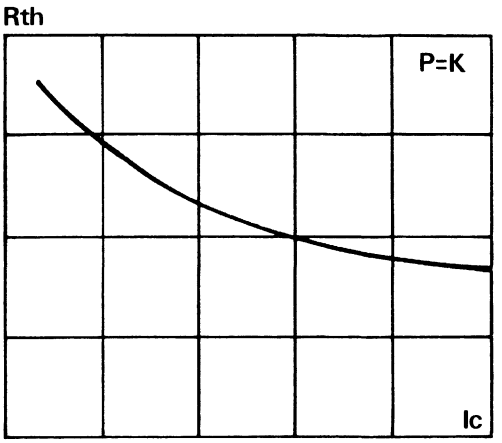


Figure 1-47 – Thermal resistance versus Ic

The conclusion which users of power products can draw from this phenomenon is that they should be especially careful when using these products at high voltage since this involves 2 potential risks:

– the risk of degradation from non-destructive hot spots.

– the risk of not having a sufficient safety margin under actual circuit conditions because of the reduction of the useable area of the chip.

The apparent variation of thermal resistance can be shown here, as a function of constant power current (i.e. in function of I/V), Figure 1-47.

A-7. Pulsed FBSOA

A-7.1. THERMAL LIMITS

A maximum ICM value is generally set equal to twice continuous IC for a portion of curves given by the manufacturers $\delta \leqq 10\%$.

For the Pmax rating a constant value with a slope of – 1 on logaritmic coordinates is used. The value of Pmax is calculated from the transient thermal impedance curves and $\delta \leqq 10\%$ (see thermal resistance).

A-7.2. LIMITS CREATED BY ELECTRIC FIELDS

Typically BVCEO is consider to be independent of temperature.

For the secondary breakdown (hyperbola ISB = kvce^{-n}) the limit is considered to decrease linearly with the tenperature, and usually at a slower rate than Pmax because "hot spots" are affected more by the electric field than by temperature.

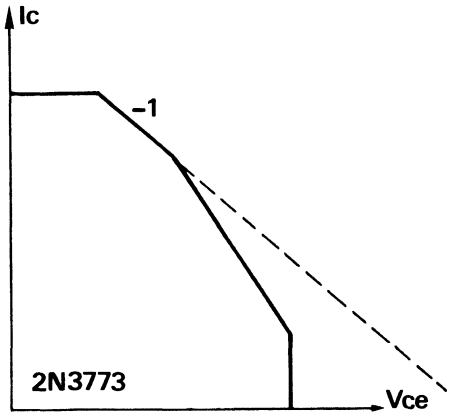


Figure 1-48: FBSOA curve

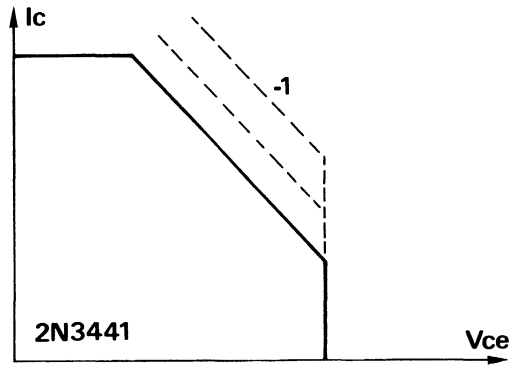


Figure 1-49 — Low voltage transistor FBSOA

When working under impulsed conditions the following methods are used analyze performance type of devices.

A-7.2.1. For low voltage device the dissipation limit is typically less than the ISB, there is no problem here, its the first limit that counts. Low voltage transistor, "Power Base" type 2N3441.

A-7.2.2. For high voltage double-diffused devices the limit for the secondary breakdown is always less than the dissipation limit, it is clearly the second BV limit which counts. High voltage transistor, double diffused type: BUT15.

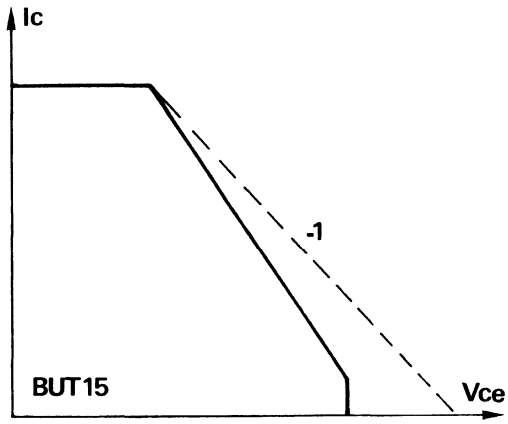


Figure 1-50 — Double diffused transistor FBSOA

A-7.2.3. In general for medium-voltage (100-500 V) power transistors, such as the 2N3773, exhibit all four SOA characteristics and are derated with temperature as shown in Figure 1-51.

A-7.2.4. In the special case for very high voltage triple diffused transistors such as the BUS48, secondary breakdown is the predominate segment as shown in Figure 1-52.

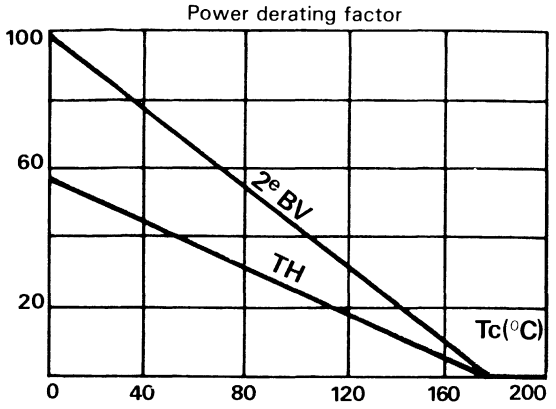


Figure 1-51 — Power derating factor

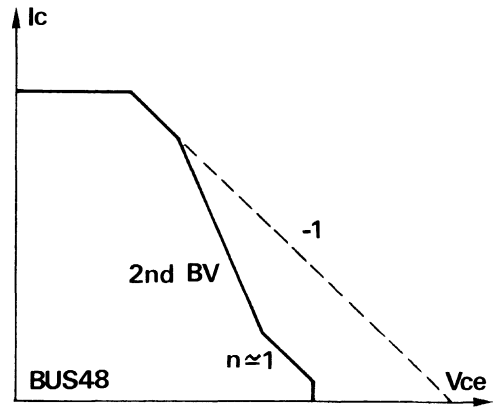


Figure 1-52 — Triple diffused tansistor FBSOA

We now see the appearance of a additional break in the 2nd BV curve for high voltages and there is a new resistance type slope with $n \cong 1$, this being attributed to widening of the base in the low-resistive N- region of the collector.

B) Switching safe operating areas

B-1. At turn off

We discussed at the end of the previous chapter the sensitivity of second breakdown at high voltages and low load currents. If this condition is maintened for negative-based currents, the phenomenon of second breakdown without the preliminary appearance of thermal instabilities always occurs. The destruction of the component is very fast, once the phenomenon occurs, probably less than a few hundred nanoseconds. However, if this behavior is analyzed closely the results shown that the mechanism is not quite identical.

Now, the electric field in the base is reversed, base current flowing through the internal base-emitter junction is forced through the center of the emitter fingers because of the edges being turned off harder than the center (see Figure 1-53). The higher the base-emitter reverse bias the higher the current density in the center.

One of the classic case on stressing power transistors during turn off is in an inductive circuit.

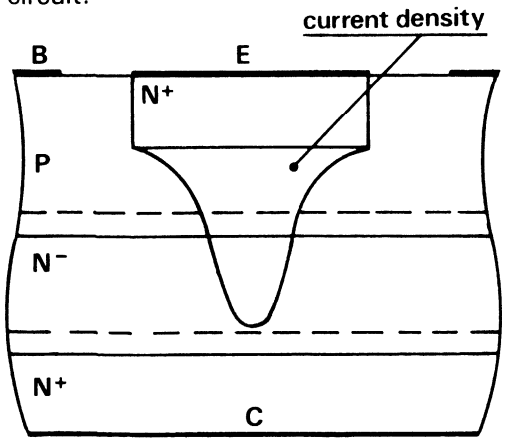


Figure 1-53 — Turn off current density

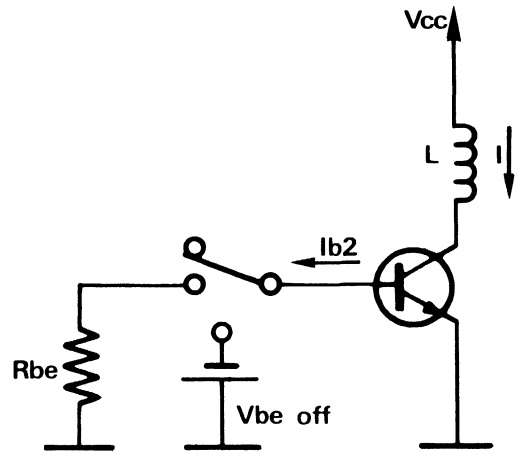


Figure 1-54 — Test circuit

In this circuit the current does not want to change instantly so the potential at the transistor VCE terminals increases rapidly approaching BVCES until the energy stored in the inductance is dissipated: $E = 1/2\ LI^2$.

In reference to the transistor capabilities, E becomes ESB (Energy Second Breakdown) and I becomes ISB (Intensity of Second Breakdown) for the specified values of **inductance L and reverse base current IBR.**

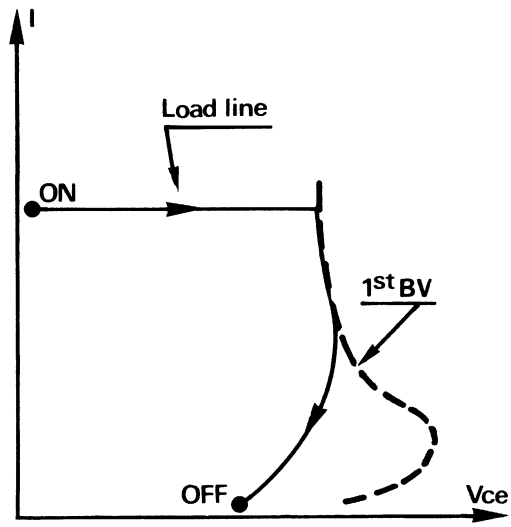


Figure 1-55 — Turn off transient load line

When IBR is higher than a certain value which gives an intersecting voltage which is greater than kT/q we can say the intensity of the second breakdown (9) is:

$$ISB_{min} = \frac{2Z^2 J_T\, kT/q}{RS\, IBR} \quad (16)$$

Z = being the emitter perimeter
RS = base resistance

J_t = critical density of current corresponding to the limit of the avalanche injection (see chapter A-5.2)

$J_t = qveND$, Ve being the speed limit of electrons in the silicon: 10^7 cm/s

From this equation we deduce immediately that the intensity of the secondary avalanche is proportional to the square of the emitter perimeter and inversely proportional to the base resistance and reverse base current (IBR).

We shall now look at the relative influence of these different parameters on the intensity of the secondary avalanche.

Let us take the case of an inductive load being turned off.

We have $V = L \frac{dI}{dt}$ and $BVcex - Vcc = L \frac{ICM}{tf}$ (17)

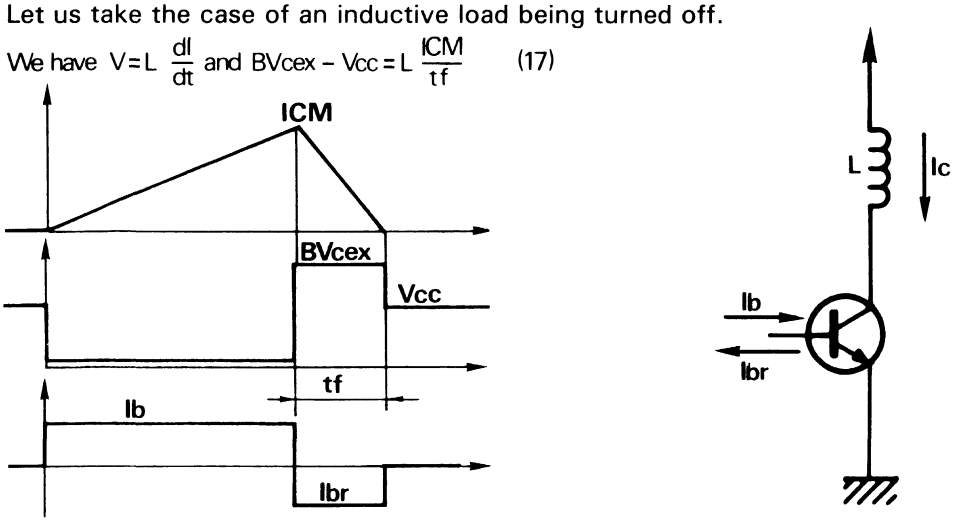


Figure 1-56 — Turn off on inductive load

Which can also be written up: $IC(t) = ICM\ (1 - t/tf)$.

B-1.1. ELECTRONIC MODEL

Supposing that L is sufficiently great to have bigger tf than the natural tf of a power component otherwise BVcex would not be attained.

If a high voltage device with low doping of N- collector is in the on state, there is an excess of minority carriers in this N- region.

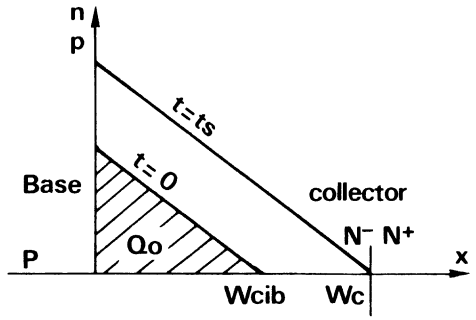


Figure 1-57

At the beginning of turn off these charges are reduced, the excess holes are removed from the base and excess electrons from the collector. Tests show that an excess of holes exists in the collector when operating at saturation (up to junction N – N) and that they must be removed before any change (Qd), occurs outside in the load circuit.

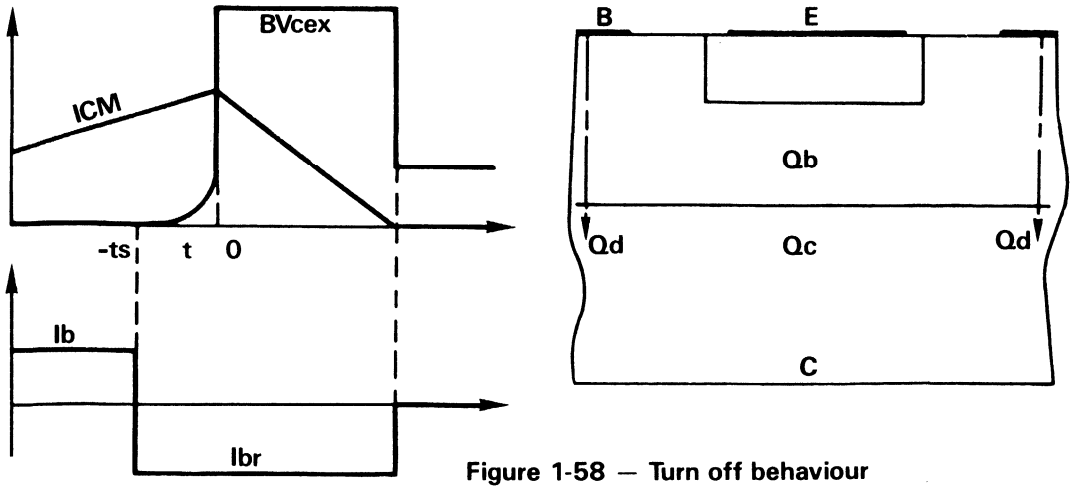


Figure 1-58 — Turn off behaviour

Figure 1-58, between time -ts and time = 0, the base current extracts Qc and Qb charges, which is part pf the amplification phenomena, VCE voltage begins to rise and the constriction of current begins to take place at the center of the emitter finger.

At time t = 0 where the collector voltage reaches BVcex, there still is a specifics quantity of charge Q (0) in the collector. One can say IBR = dQ(0)/dt.

After a specific time τ, there is no longer any stored charge and the load current begins to decrease.

$\tau = Q(o)/IBR$ (18) This can also be written as $ICM = Q(o)/t_{cib}$ (19) with $t_{cib} = 4\frac{W^2 cib}{DC}$

DC being the diffusion coefficient of minority carriers in the collector.

The charge Q(t) excess is important because it reduces the value of base resistance RS (eq 16) during fall time $0 < t < tf$, Q and IC decrease linearly with time the condition $\tau < tf$ implies that Q reaches zero before the load current.

In this case, a second breakdown may arise if $Ic(\tau) > ISBmin$. when a component is tested for second breakdown energy, the IBR is fixed and ICM is increased just until this phenomenon is produced for a reverse base current fixed at IBR, charge recovery time is: $\tau = ICM\ (tcib/IBR)$ (20)

The equations 18 and 19 come from the slope line ticb/IBR in the plane ICM = F(t). Therefore the collector current IC (τ) values for which the constriction arises are located in the mixed line on this graph.

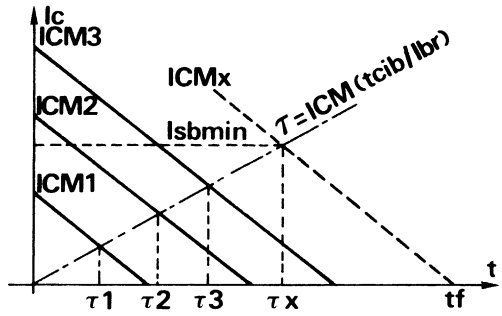


Figure 1-59 — Maximum current versus time

ISB min is obtained from equation 16 can be shown also we can see that collector currents ICM1 $<$ ICM2 $<$ ICM3 do not lead to the secondary avalanche as IC(τ1) $<$ IC(τ2) $<$ IC(τ3) $<$ ISB min.

The secondary breakdown will arise for an ICM(x) current value which will give a value IC(x) = ISBmin for maximum constriction.

But when testing the device the value of the intensity of secondary breakdown is ICM(x) therefore we can write:

$ICM(x) = ISBmin / \left(1 - \frac{\tau x}{tf}\right)$ and $ISBmin = ISB\left(1 - \frac{t}{tf}\right)$, from the equation 17

we have tf = ICM/(BVcex-Vcc), from

the equation 20, $t = \tau = ICM(tcib/IBR)$ so $ISB = \frac{ISBmin}{1-L_1/L}$ (21) if we say that $L_1 = \frac{tcib(BVcex-Vce)}{IBR}$

This equation indicates that the intensity of the secondary breakdown increases as load inductance decreases to value L1 = L where it is theoritically infinite.

Values of inductance L less than L1 imply that τ is greater than tf, which shows that pinching does not occur during current fall tf; and RS remains modulated by conductivity.

One can say that at this point, the secondary breakdown does not occur because of avalanche injection, but because of thermal effects which we shall now study.

B-1.2. THERMAL MODEL

If we assume that all the energy stored in the inductance changes into heat in the transistor and causes the temperature of the active region of the power transistor to increase diabatically, then for an identical temperature, we get a secondary breakdown constant energy of: $ESB = \frac{1}{2} L\, ISB^2$ in the ISB = F(L) graph we have: $ISB = k\, L^{-1/2}$ thus a $-1/2$ slope line on logarithmic co-ordinates.

B-1.3. GENERALIZATION OF MODEL

The model will have a particular point L = L1 defined by the physical parameters of the power component and base control.

B-1.3.1. If L$<$L1 it is possible to have a second breakdown by thermal effects for a constant energy.

B-1.3.2. If L$>$L1, second breakdown by injection on the ISB = F(L) graph, gives:

$ISB = \frac{ISmin}{1-L1/2}$ i.e. a hyperbole, Figure 1-60, approaching ISB = ISB min

If we make curve E = F(L) we get Figure 1-61.

the first part up to L = L1, we have E = constant, then by making L = kL1, we obtain:

$E = \frac{1}{2(k-1)^2} \frac{k^3}{L_1} ISBmin$ which has minimum a value for k = 3 and infinite for K = 1, for K = 10, if we assume a 10% error, we get E = kL1 ISBmin.

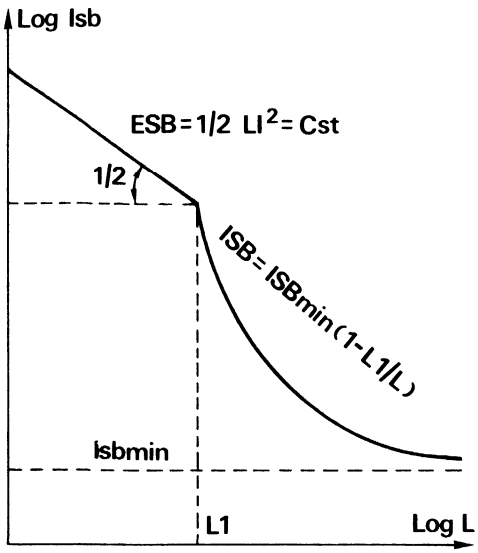


Figure 1-60 — I_{SB} versus inductance

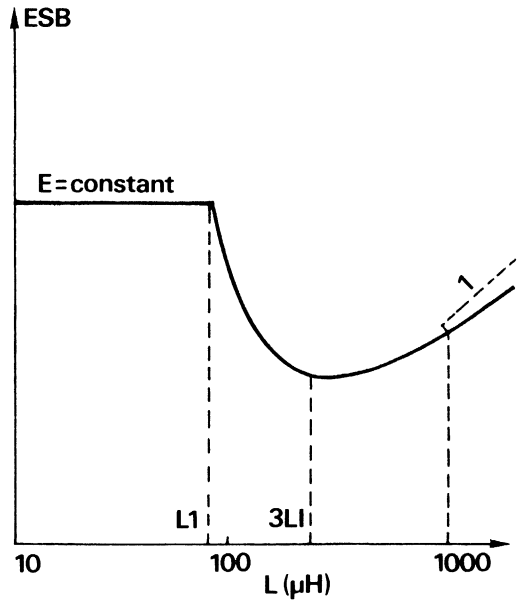


Figure 1-61 — E_{SB} versus inductance

B-1.4. Charges in secondary breakdown verses RBE and VBE (off) we have seen ESB = F(L), we must now look at ESB = F(VBE,RBE).

The ISB formula (16) indicates that ISB varies inversely with IBR. At RBE = constant, if VBE (off) increases IBR rises then ISB and ESB decrease.

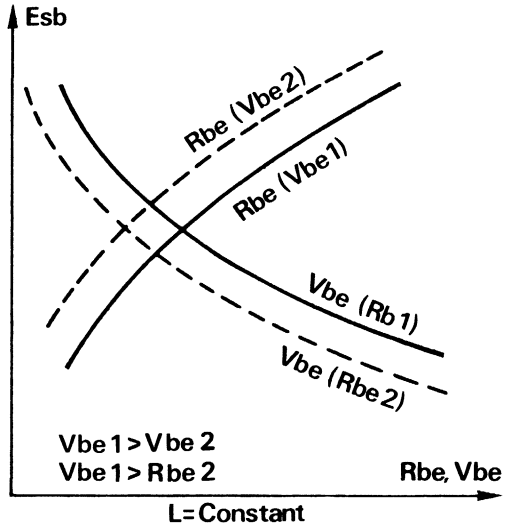


Figure 1-62 — E_{SB} versus Rbe, Vbe

In the same way, at constant VBE, if RBE increases, IBR decreases and ESB increases. All of this at constant inductance L (Figure 1-62).

B-1.5. CRITIQUE OF MEASURING THIS PARAMETER

Even if we measure the energy of the secondary breakdown for a power transistor with a non-destructive circuit, it seems clear that this attempt endangers its reliability. It is also clear that the maximum energy the transistor can support before secondary breakdown is very sensitive to the value of the circuit inductance.

Finally, the energy capability decreases when IBR is increased, however IBR is typically increased to improve switching times and thus reduce losses in the power transistor. Reducing the temperature improves long term reliability.

It would seem that the best approach is not to drive the transistor into secondary breakdown to prevent this the power transistors must be protected either by a zener or by a protection circuit (see following chapter).

The performance of the power switch is voltage-protected or clamped is different than the performance we have just looked at and will be described in the following paragraph.

B-1.5.1. Reverse bias safety operation area (RBSOA)

The test is performed by using the circuit shown in Figure 1-63.

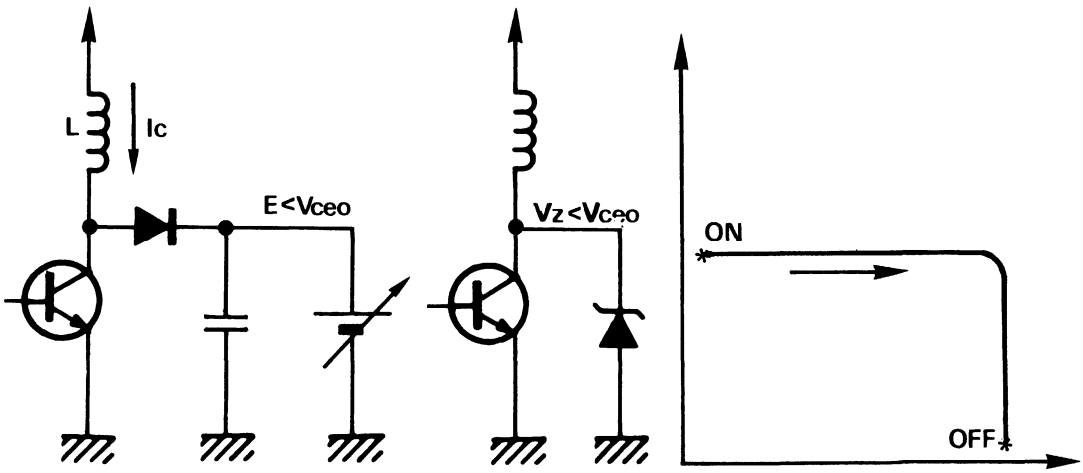


Figure 1-63 — RBSOA test circuit

Which represents a more typical application than the unclamped inductive switching circuit. This circuit can be designed to be non-destructive and to have no effect on the long term reliability of the device being tested.

The points where the secondary breakdown begins are shown in Figure 1-64.

The relationship is shown for different values of reverse base current IBR = IB2 there are two main sections for these curves.

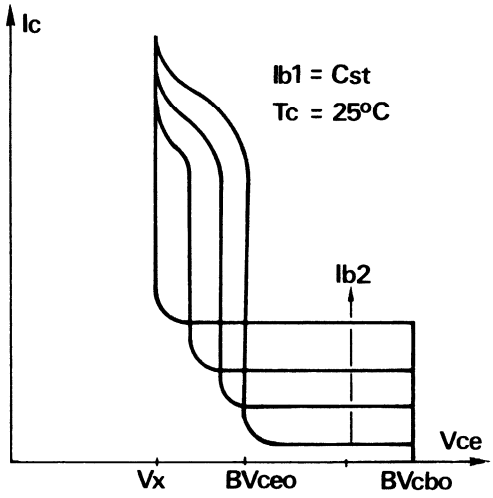


Figure 1-64 — 2nd BV limits

B-1.5.2. A vertical section, varying very little with IBR. We have an avalanche injection phenomenon here: high current density (100 to 1000A/cm²) and strong electric field (VCE≅VCEOSUS), the critical field moves to toward the N−N+ junction (see paragraph A-5.2). The instable area tends to reduce itself to a small spot at high temperature (500 to 600°C) at the center of the emitter finger and quickly destroys the device.

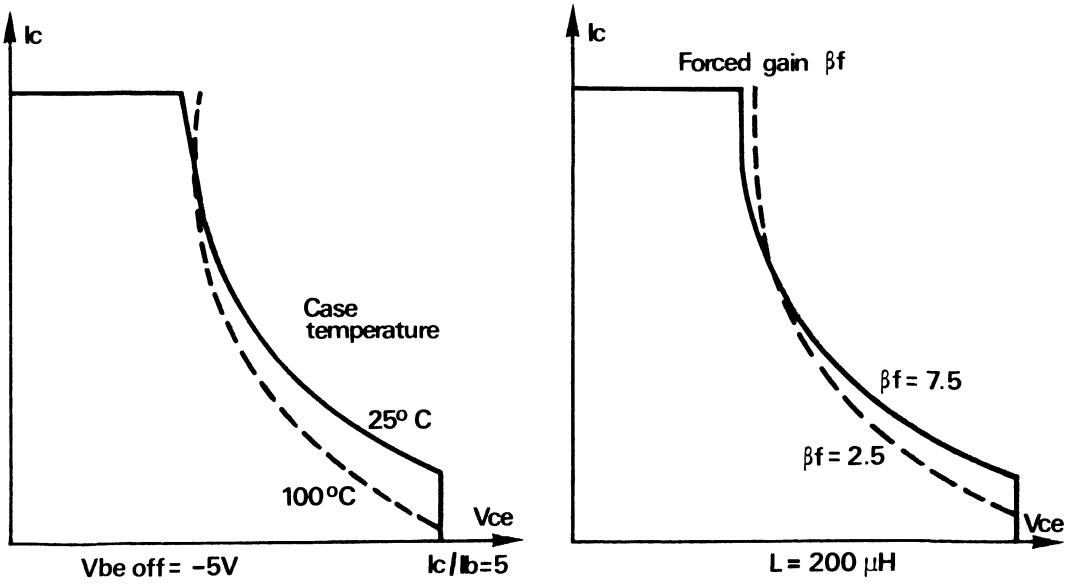


Figure 1-65 — RBSOA versus T°, Bf

B-1.5.3. A more or less horizontal section at lower currents. At this point most of the avalanche injection current is removed by means of the reverse base drive. If this removal is large enough the secondary breakdown capability will be increased even at righer voltages.

The second beakdown mechanism can be explained in this region by the increased conduction of small transistors near the center the emitter finger at the moment of turn off. Which is a result of high base current and internal base resistance.

In Figure 1-65, the changes in RBSOA capability are shown as a function of temperature and forced gain we note on the first curve that RBSOA decreases predominately at low currents when the junction temperature increases.

On the second curve, we see a similar characteristic, the RBSOA decreases at low currents when the transistor is highly saturated before turn off ($\beta F = 2.5$).

The accumulation of carriers under the center of the emitter fingers explains this variation.

B-2. Safe operating area at turn on

In most inductive circuits, the current and voltage waveforms during turn-on are similar to those shown in Figure 1-66.

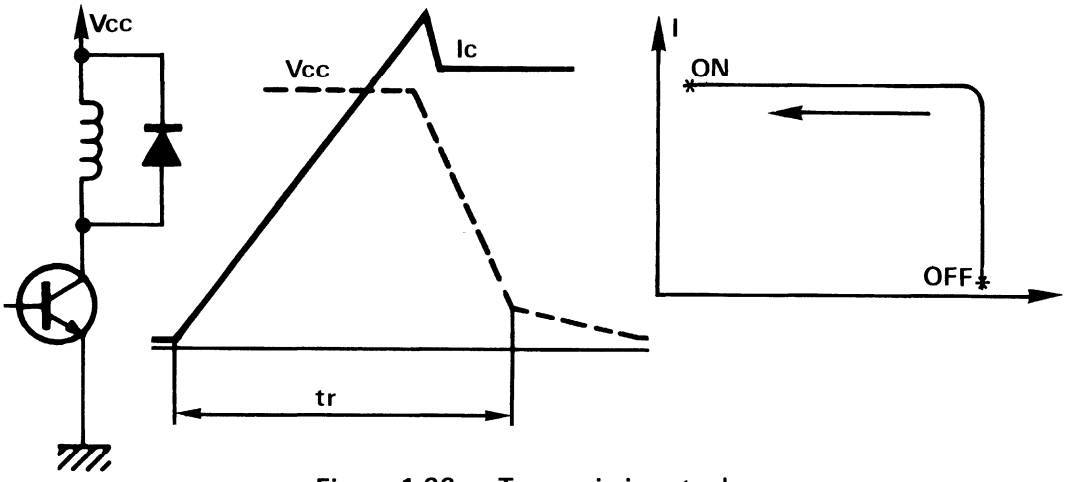


Figure 1-66 — Turn on in inverter leg

The turn-on load line appears to be identical to the turn-off load line, but the devices has much more capability in terms of secondary breakdown for the forward biased condition that it does for the reversed biased condition. This is due to the fact that during turn-off the current is forced into a small area at the center of the emitter, as oppose to turn-on where the current is forced to the edges of the emitter fingers and the same current density is spread out over a larger area.

If we use a controlled base drive at turn on: Ibl at turn on equal to 3Ibl at turn off and a dIbl/dt as large as possible, we avoid excess heating since the turn on losses are proportional to turn on time t_r and the secondary breakdown region is traversed quickly (vertical part of safe operating: less than 100 nanoseconds).

This result in a lower probability of destruction due to secondary breakdown. Finally the off condition is determined by the value of supply voltage, which should be lower than the BVceo of the transistor. The load line should lie within the boundaries of the RBSOA curve as shown in Figure 1-67.

The BVcew is typically set at BVceo for discrete and darlington, however, the BVceo rating of a darlington typically includes internal resistors and is in reality a BVcer rating.

For turn on with a supply voltage higher than BVcew, the boundary of current at a specific BVceo can be increased by factor 4 or 5 if this region is traversed quickly, typically less than 100 nanoseconds. Recent test indicate that this can be done with any degradation to the device.

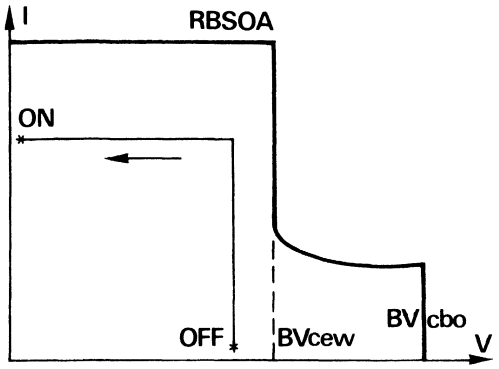


Figure 1-67 — Turn on load lines

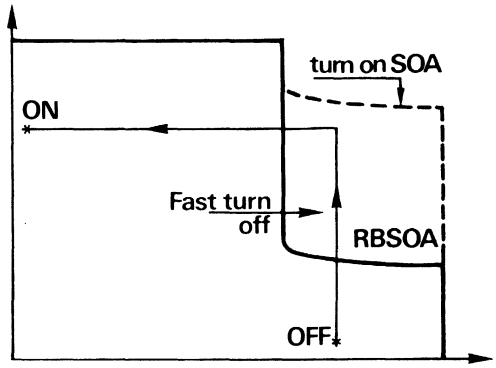


Figure 1-68

C) Overload safe operating areas

(OLSOA: overload safe operating area).

There are two typical applications where overload currents may exist (maximum overload).

The external circuit fixes the Ic current in the collector: this is **the most common case** (i.e. inductive circuits).

The circuit has zero or low resistive inductance (dIc/dt may be infinite) in this situation the transistor gain fixes the short circuit current. $Icc = \beta I_B$ for the power switch itself two conditions may exist: when a temporary overload current occurs, the device remains in saturations. In this case, the transistor is very strong and can sustain many times its maximum current rating may which reach 5 times I nominal.

General case: the overload is permanent: when the device senses condition, it begins the power circuit may be opened by saturation and can reach: $Vce = V\text{supply} + LS \frac{dIcc}{dt}$

LS being the parasitic inductance due to wiring.

The LS dIcc/dt value may be very high because the device takes a certain amount of time to react and the transistor has a non-negligeable storage time, which means the Ice may be high or equal to 2 I nominal, turn off time $tf = dt$ is very fast which results in the device pulling out of saturation and Vce rising very rapidly as shown in Figure 1-69.

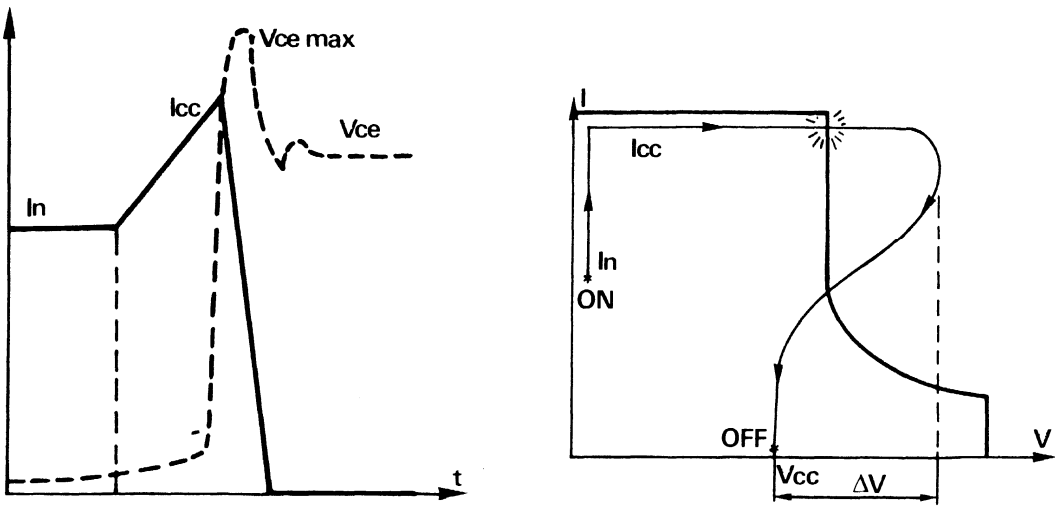


Figure 1-69 — Short circuit transient load line

Refering to Figure 1-70 the overload safety areas will be of two types:

C-1-. OLSOA I

Is measured in a common base circuit which allows precise definition of collector-emitter voltage and collector current.

C-2. OLSOA II

Applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor.

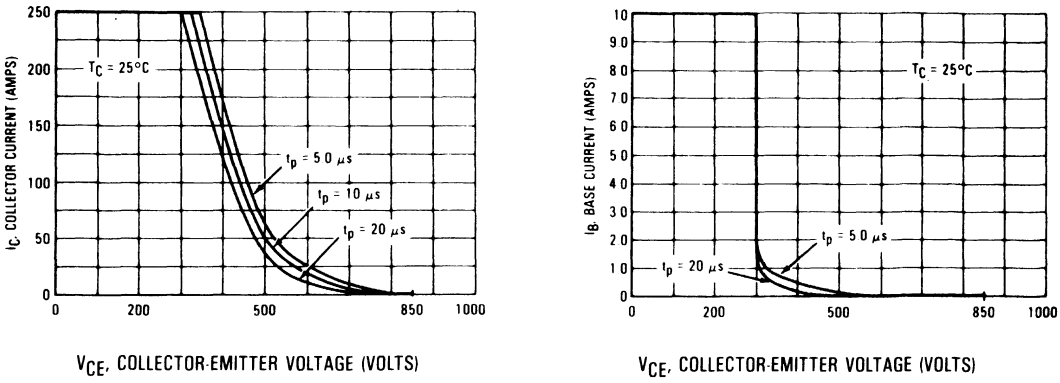


Figure 1-70–Overload safe operating area type I and II (OLSOA)

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Various Power Switches Technologies

Section 2

TABLE OF CONTENTS

1. Bipolar products

A) Darlington

A-1. Technology

The Darlington, was named after its inventor and is the cascade combination of two transistors to obtain gain multiplication, see Figure 2-1.

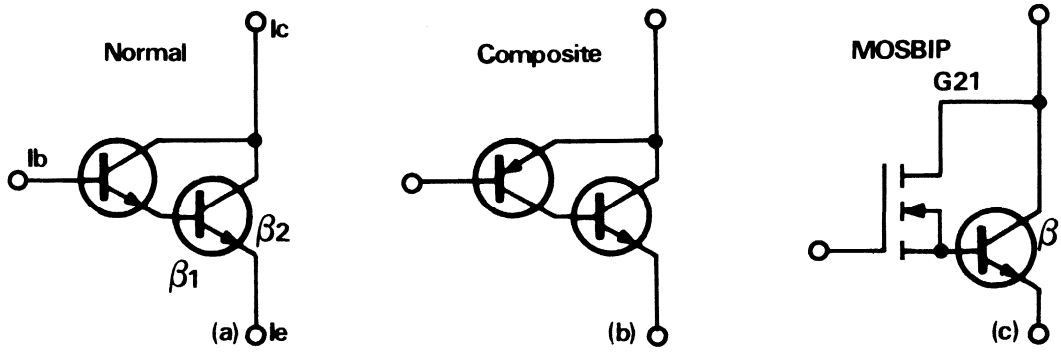


Figure 2-1

If we call system gain GS = output/input we have in the 3 cases: a) $\beta D = \beta 1 \cdot \beta 2 + \beta 1 + \beta 2 = Ic/Ib$ b) $\beta D = \beta 1 \cdot \beta 2 + \beta 1 + 1 = Ic/Ib$ c) $GS = g21 \times \beta = Ic/VG$
We normally take: $\beta D = \beta 1 \cdot \beta 2$ or $g21\beta$
These combinations were originally constructed with "discrete" elements. Following their success, manufacturers started producing hybrid Darlingtons in a single packages, then, to improve production costs, monolithic products were developed.

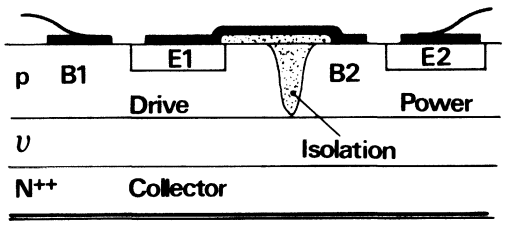


Figure 2-2 – Darlington

A parasitic resistance R1 occurs, because of the base combination of the 2 basic transistors: Figure 2-3.
This resistance must be as high as possible so that the device gain is not significantly reduced.

R2 is needed to provide a path for the leakage current of the drive device it does not provide excess base drive to the output device when the Darlington is in the off condition.

To construct this resistance inexpensively, the designers of semiconductors decided to use the silicon resistivity.

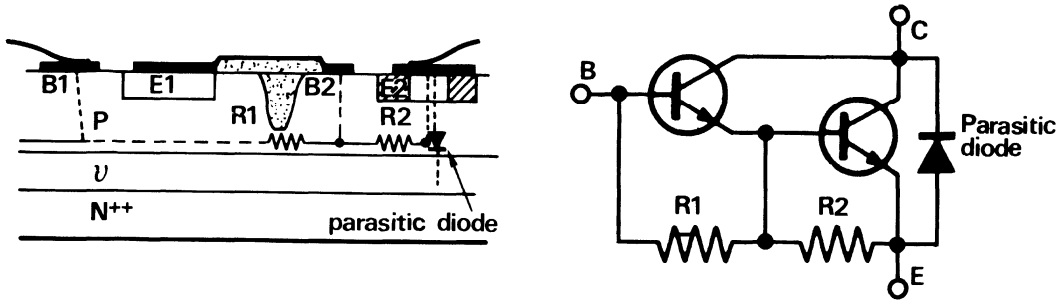


Figure 2-3

Unfortunately, the window in the emitter which provides the resistance contact of the P base layer for resistance R2, also creates a parasite diode at the emitter contact, through the P base region and N region of collector.

Darlingtons were first used in linear systems and this kind of construction is sufficient for this type of application. The question now is whether the Darlington structure works well in recent application of power products: **the switch.**

When the Darlington turning off, the removal of base current should be simultaneous from both transistors to have effect turn off.

Unfortunately, the R1 resistance, through which carriers are removed for the output device has a high value and restricts effective removal of charge if a diode is inserted between the 2 bases, then the charge can be removed rapidly. This diode is called a "speed up diode"- SUD.

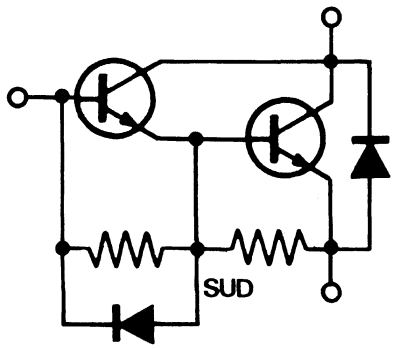


Figure 2-4

There are two ways to do this monolithically if the input transistor silicon is used, there is, unfortunately a parasite thyristor created by the four successive layers p n p n.

To avoid latching of this parasitic thyristor ($\alpha 1 + \alpha 2 = 1$), the size of r must be reduced as small as possible and the composite transistor gains reduced $\alpha 1$ and $\alpha 2$ so that the latching state is not reached.

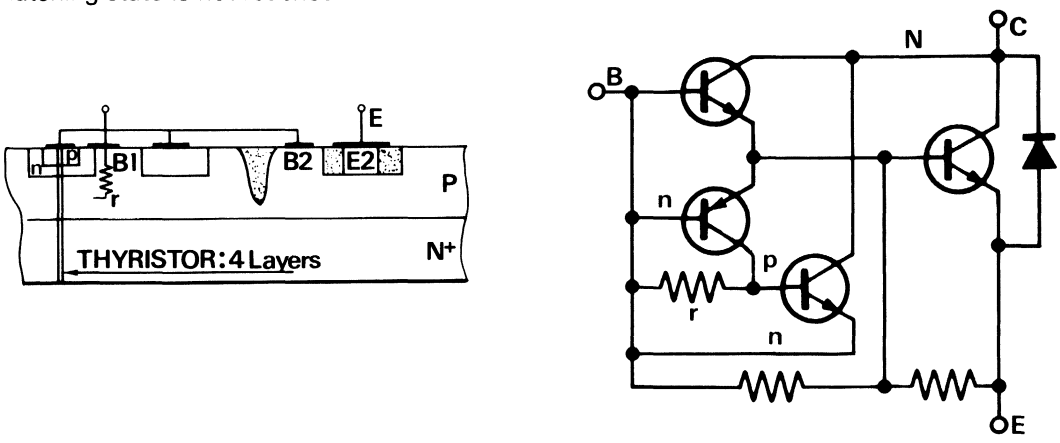


Figure 2-5

If the output device silicon is use for this SUD, a parasitic transistor is created which is not optimised for safe operating area at turn on and is therefore weak.

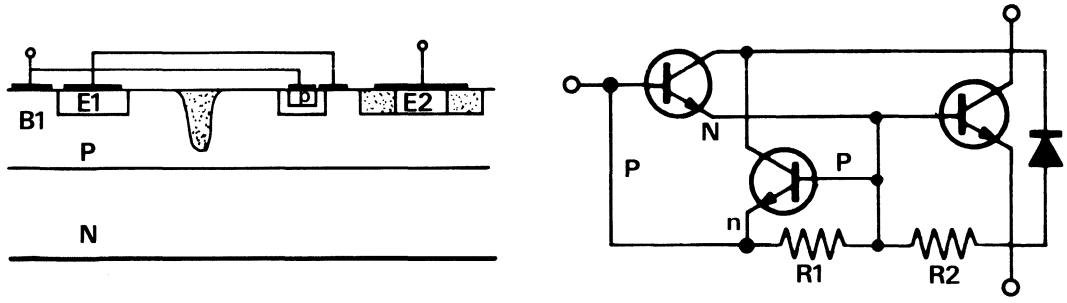


Figure 2-6

So, to avoid the problems of diffusion many manufacturers often choose to add a separate discrete diode in hybrid form. However, some packages such as the TO-220 and TO-218 (TO-3P) do not lend themselves to this type of construction. (Restricted space and difficult to make connection.)

We have already seen that the R2 resistance creates a parasitic diode between the Darlingtons collector and emitter: also called a free wheeling diode. This is unfortunately not optimised as fast diode, i.e. reverse recovery time trr is slow.

It is always difficult to physically optimize a particular function without affecting the total function: in solid state physics, we are always confronted compromises:

- speed – voltage
- gain – voltage, etc...

So that, power semiconductor manufacturers would prefer to leave this parasitic diode out of the chip design and add a hybrid freewheeling diode when the package permits and the application requires a faster diode.

The question which needs asking now is: are R1 and R2 resistances necessary for these switching products and if not, how can they be omitted? An R1 resistance is not necessary for a monolithic Darlington but is the result of the metallic emitter-base connection of the 2 transistors across a mesa. The only solution would be to use planar technology. The Darlington is mainly used in high voltage applications to compensate for the reduced gain that is associated with increasing the voltage capability of the devices.

$$\text{i.e. } hFE = \frac{K}{(Vcesus)^{2.3}}$$

There are many applications where mesa technology is preferred for other characteristic making it difficult to remove R1. Another alternate for mesa devices is to make the value of R1 as high as possible and still compatible with the technology. The answer for the R2 resistance is a little more difficult a certain number of controls are needed, which are discussed in the following chapter.

A-2. Characteristics of Darlingtons – Advantages – Disadvantages

A-2.1. The main advantage of this configuration is to improve silicon efficiency for a specific voltage/current/gain requirement.

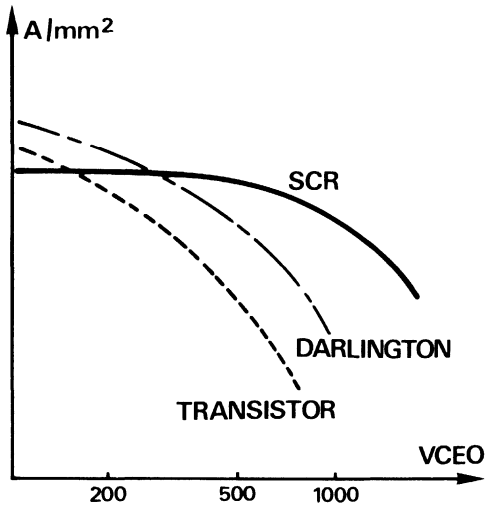


Figure 2-7

With the same package and the same amount of silicon, i.e. practically identical parts costs, the Darlington is the best compromise for: gain – speed – voltage.

Let us look at two products with identical voltage and speed:

– the BUS48 discrete with 35 mm² of useful area and peak pulse power capability of Ic × Vcew i.e. 15 × 300 V = 4500 W.

– the BUT15 Darlington with 27 mm² of useful area and peak pulse power capability of 20 A × 300 = 6000 W.

The Pc/A efficiency is thus 130 W/mm² for the BUS48 and 220 W/mm² for the BUT15.

A-2.2. SWITCHING SAFE OPERATING AREA FOR DARLINGTONS

It is a common belief that Darlingtons exhibit lower safe operating area capability than discrete products however when comparing the RBSOA capability of modern day devices with the same die size it can be seen from Figure 2-8, that this is not necessarily so.

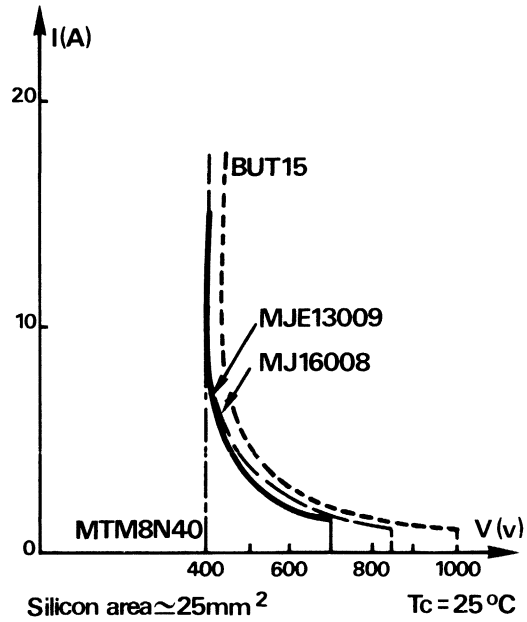


Figure 2-8

A-2.3. PARALLELING DARLINGTONS

What are the criteria for good paralleling?

- Very good thermal connections
- Symetrical wiring
- Equal sharing of Ic = F(VBEON)
- Close matching of storage times

The first 2 demands are valid for all types of semiconductor. How do the last 2 compare with discrete transistors?

The transconductance curves for two known devices, the MJ10051 Darlington and the BUS48 are shown in Figure 2-9.

From these curves, we see that the change in Ic for a maximum change in Vbe(on) is about 20% far a Darlington verses about 30% for a discrete, giving the Darlington an advantage when paralling devices.

What about storage times? If we take a Darlington with its speed-up diode (SUD), we see from Figure 2-10, that the Darlington has a natural Baker clamp (see chapter on environment of power transistor). The advantage of this is that it decreases ts (storage time) and helps to reduce the possibility of mis-matched devices when paralleling.

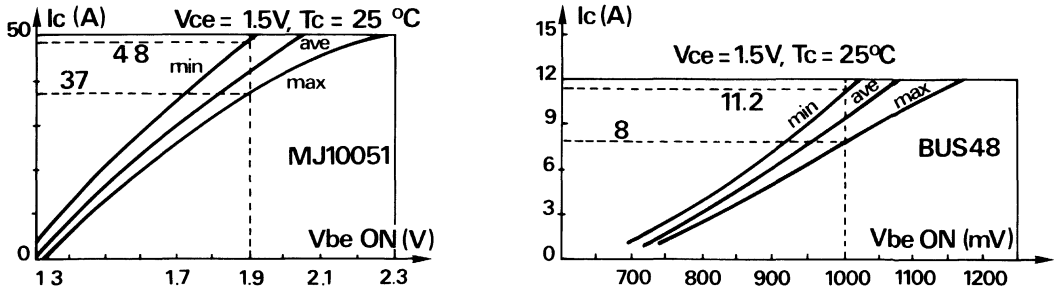


Figure 2-9

Another possible problem in paralleling Darlingtons with speed up diodes can be see from analysing in Figure 2-11.

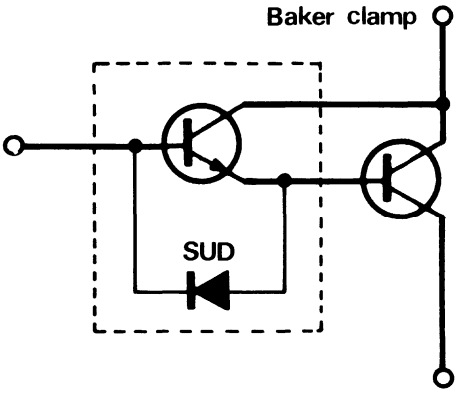


Figure 2-10

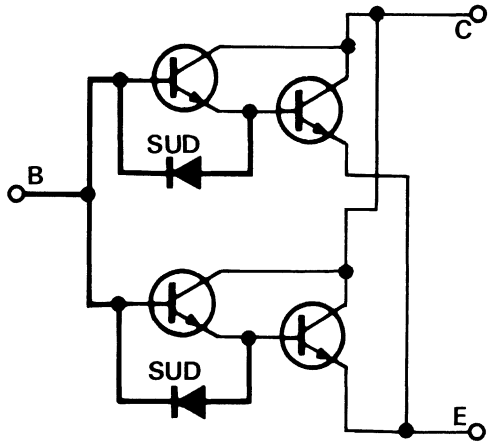


Figure 2-11

In this configuration the base-emitter junction and SUD of one output device is in parallel with the base-emitter junction and SUD of the other output device. If one diode stays longer time than the other. A mis match of Ic could occur. However the turn-on time for these diodes are very fast, several tens of nanoseconds, which is small compared to the storage time for a bipolar.

To conclude this section, we can say, and experience shows that, paralleling Darlingtons is at least as easy and safe as paralleling discrete transistors.

A-2.4. WHAT DOES THE DARLINGTON ADD TO APPLICATION EFFICIENCY?

A-2.4.1. If we look at turn on losses for a convertor (with freewheeling diode) we know that first part of the current rise at turn on is determined by the switching device:

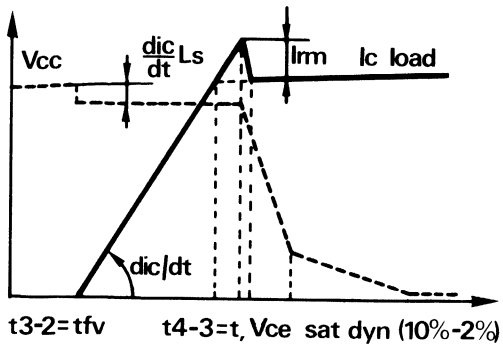


Figure 2-12

dIc/dt A/μs	Product
100	Discret BUS48 SM II
500	Discret switchmode III
600	Darlington switchmode I

Table 2-1

The first part of turn on losses (30 to 40%) is inversely proportional to dIc/dt losses = 1/2 V. Ipic² × dt/dIc

A Darlington thus has intrinsically lower losses at turn on than a discrete product.

A-2.4.2. What are the conduction losses of a Darlington used as a fast switch?

If a comparison is made with a discrete device, it is clear that for a large part of the utilization curve, the discrete has the advantage.

However a discrete product with Baker diodes is often used, making the advantage less clear.

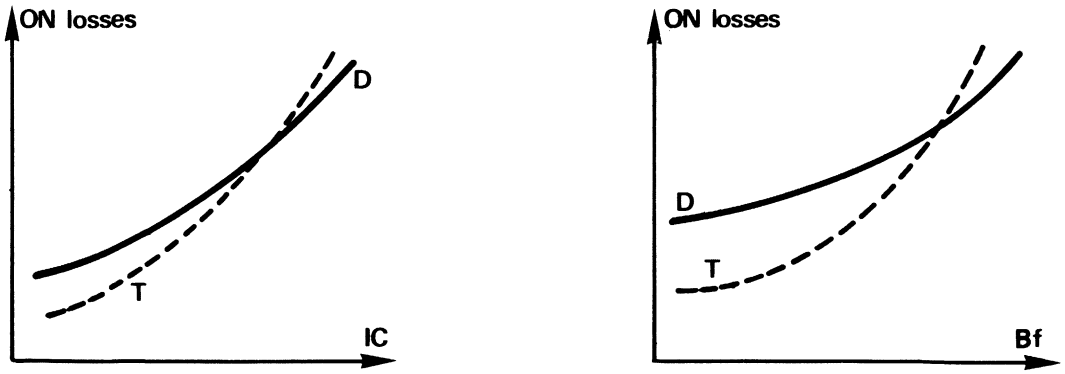


Figure 2-13

A-2.4.3. Losses at turn off

Looking at these 2 graphs, we can say that in a wide range of applications, the Darlington is at least as good as the discrete with corresponding technology in terms of losses at turn-off.

To conclude, for total losses, we can say that the Darlington is at least as good as the discrete: in high voltage applications the losses in the control circuit typically increase because of the reduced gain of the available devices. In this situation the Darlington's higher gain becomes advantageous.

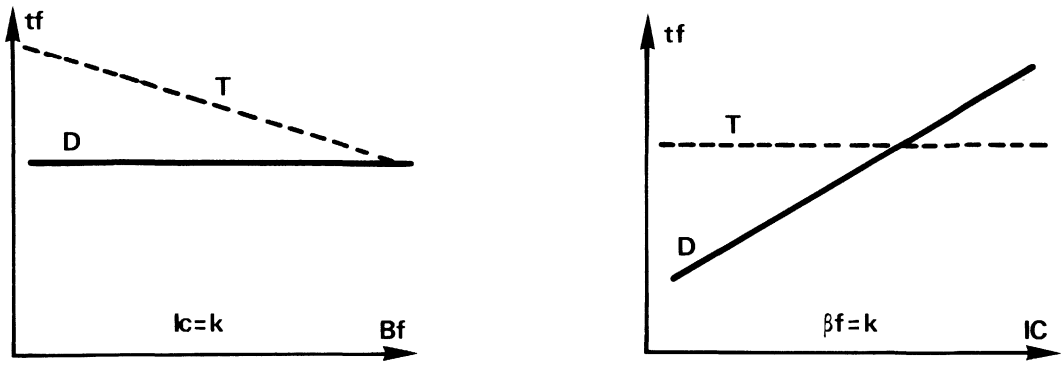


Figure 2-14

A-3. The Darlington of the future

By studying different switches, we can that the Darlington would be used as a first choice for high voltage, high power, switching applications.
New products are being developed to fit these growing applications.

A-3.1. THE FREEWHEELING DIODE AFFECTS
Example: MJ10050 Darlington 50A · 850 V with monolithic diode and the MJ10051, same device but with a separate hybrid diode.

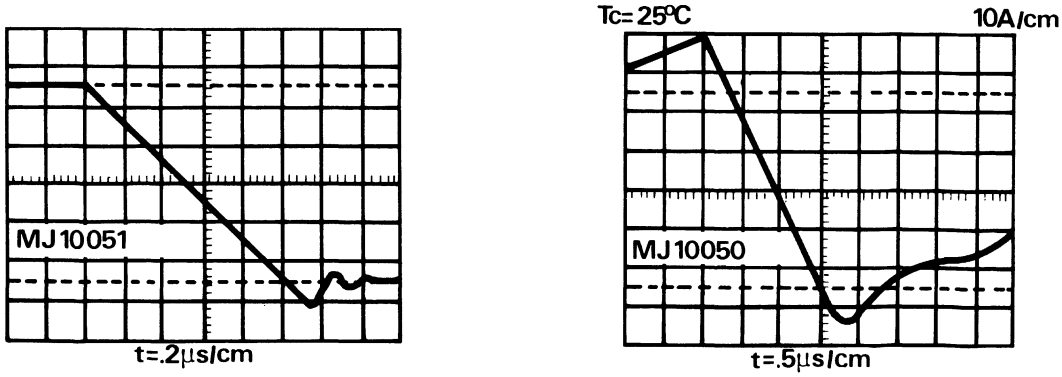


Figure 2-15 – Trr freewheeling diode

These oscillograms speak for themselves.
The short circuit time and the current flowing through the device, commuted in the "totem-pole" prohibit the use of a device with a monolithic diode.

Removal of this diode occurs automatically with removal of R2 resistance. The time has come to question the usefulness of this resistance.

A-3.1.1. Removal of R2

Thermal stability. This resistance was used to guarantee the thermal stability of Darlingtons used in linear amplification. For switches, when the product is off, there is either:

- a negative voltage on its base, or
- an emitter base drive loop with low impedance in order to guarantee the switches immunity to parasitic and large dV/dt. The leakage currents are not troublesome as they derive from the emitter base junction of the power section. So R2 can be omitted.

A-3.1.2. Inverse conduction

We know that with an inverter leg, that is freewheeling, a section of load current can pass in reverse through the Darlington because of the relatively high V_F of the freewheeling diode.

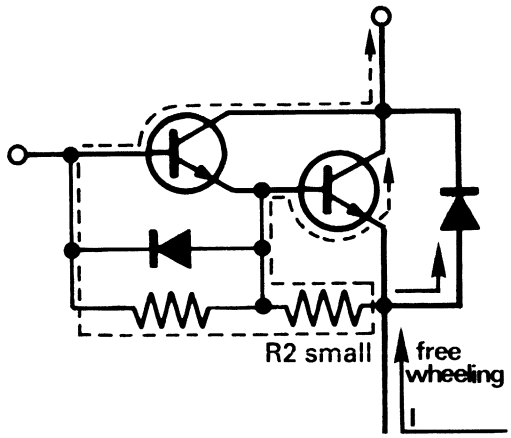
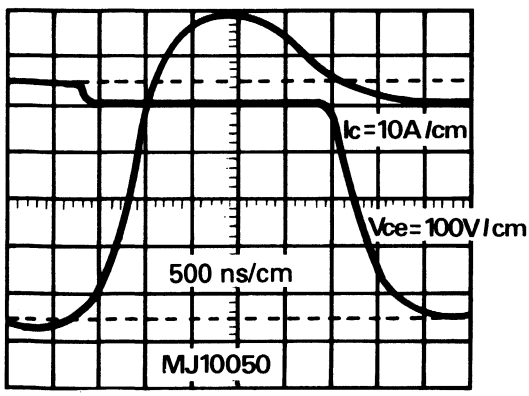


Figure 2-16

Turn on with parasitic diode



Turn on with fast MR5108 in freewheel

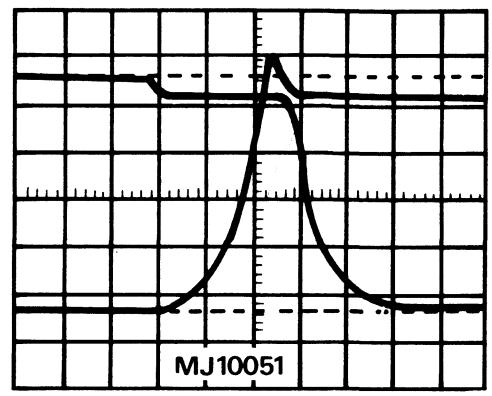


Figure 2-17

And we get a very high overload current for the device in series in the "totem pole" the next time it is turned on. This system would also be very dangerous for the life of the device if operated in reverse conduction.

For this reason also, the removal of R2 is desirable.

A-3.1.3. dV/dt during the off condition.

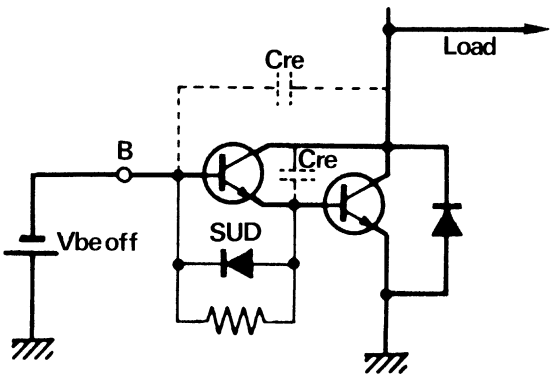


Figure 2-18

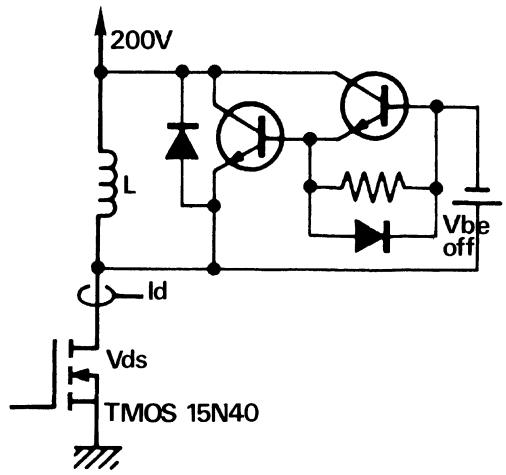


Figure 2-19

For this inverter leg application, if the top switch is controlled by pulse width modulation, the device shown receives from the device above during each cycle, a dV/dt which can be high, i.e. 1 kV per microsecond. As the Miller Cre capacitance between collecter and emitter is larger in this type of product, we can have a capacitive current of: $I = C\,dV/dt = 4\ 10^{-9} \cdot 10^{9} = 4A$ for a capacitor of 4 nanoFarads.

The question to be asked then is: "What is this current going to do?"

With an R2 resistance, we have a current which circulates in the drive loop during the off condition: I = VBEOFF/R2 and as a result in the SUD, when a parasitic current comes along, it flows directly towards the source without driving the output device into conduction.

If R2 is absent, the SUD is not permanently ON, we reduce the reverse current during of condition but what happens at the moment of dV/dt?

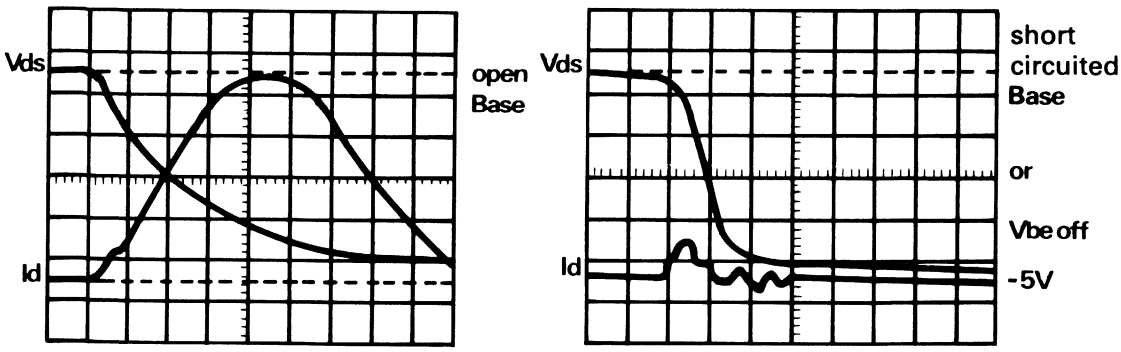
To answer this question, the following test has been made: Figure 2-19.

The Darlington to be studied is negatively biased. A low duty cycle is chosen to avoid the phenomena of inverse current or trr which superimposes itself on the actual current because of high dV/dt: Figure 2-20.

We can now say that with dV/dt attaining 1750V/microseconds there is no dangerous reconduction phenomenon whether or not R2 resistance is present.

The second potential problem resulting from the absence of R2 is the possible breakdown of the emitter base junction of the Darlington output section caused by the Vdyn of the freewheeling diode: Figure 2-21.

With R2



Oscillograms for MOS control device

Without R2

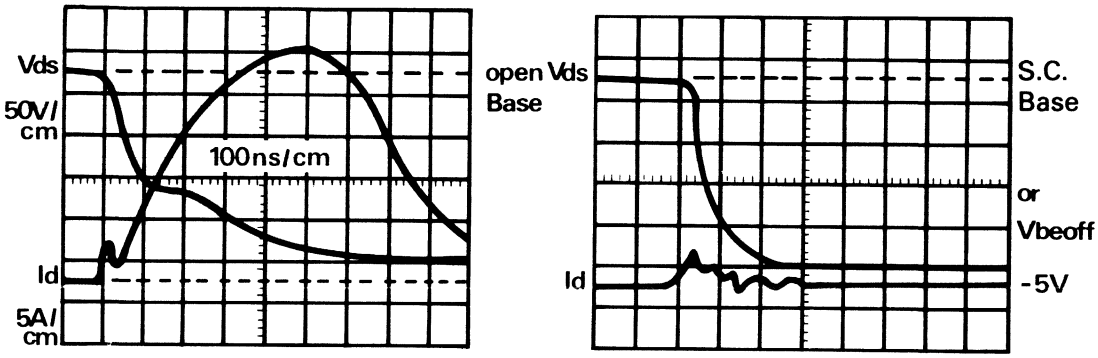


Figure 2-20

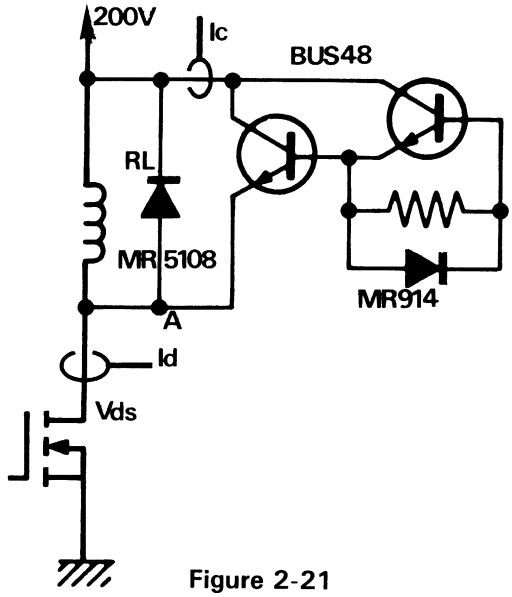


Figure 2-21

To test this phenomenon a discrete Darlington was built with switchmode II (BUS48) products with a silicon area identical to the MJ10051.

At this point a current probe can be used as indicated in the previous diagram.

When the MOS device opens, a freewheeling current tries to establish itself through the R_L diode. This, like all diodes, shows an inductance effect due to the connections and the product itself. This means that at the time of opening the MOS device, there is an overvoltage at A due to the Vdyn of diode R_L. This overvoltage is generally of about ten volts during one hundred nanoseconds. Any output section emitter-base junction having less than 10 V, would breakdown; thus leaving a current in the probe.

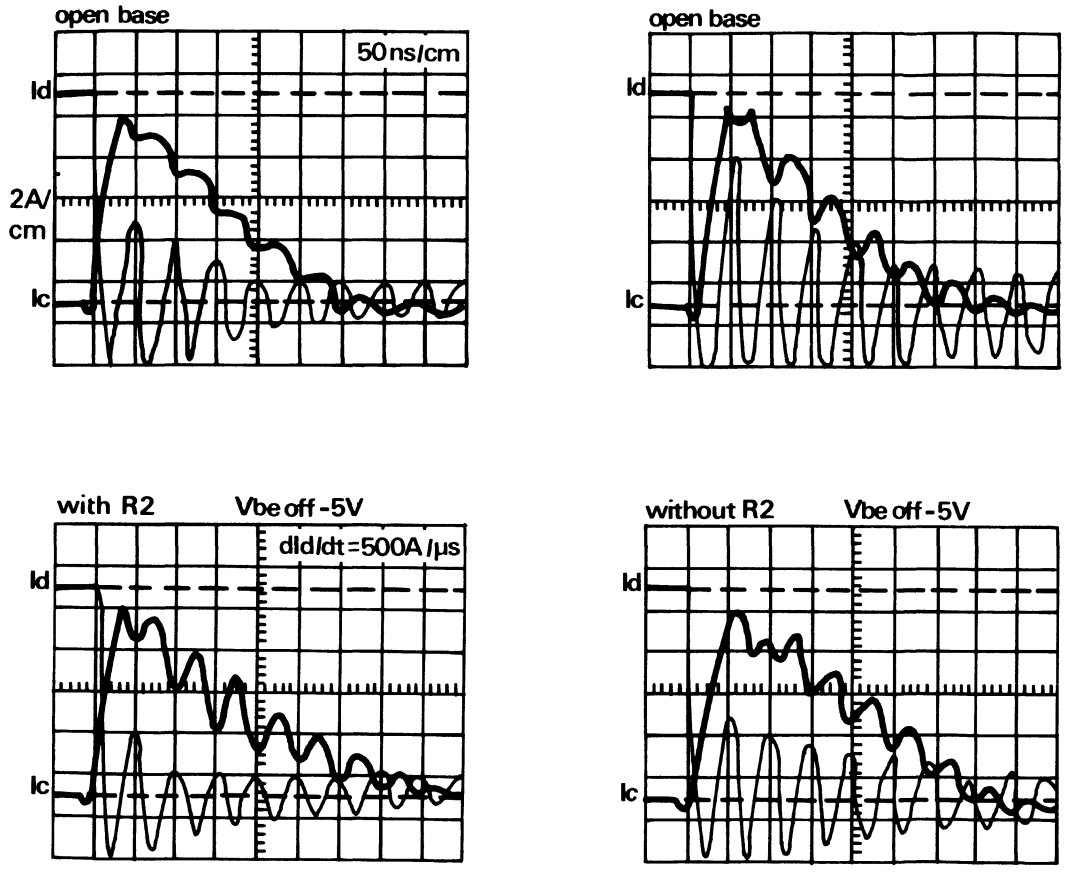


Figure 2-22

We can see then that the presence or absence of R2 in no way modifies the fact that the product avalanches BVebo for several hundred nanoseconds. We have seen, elsewhere, that this phenomenom in no ways affects product reliability.

To check that there is no additional phenomenom, we included a diode in series: Figure 2-23.

To conclude the question of the usefulness of the R2, we can now say that its absence is totally beneficial both in assembly and to the device itself.

We can now speculate on the Darlington of the future: Figure 2-24.

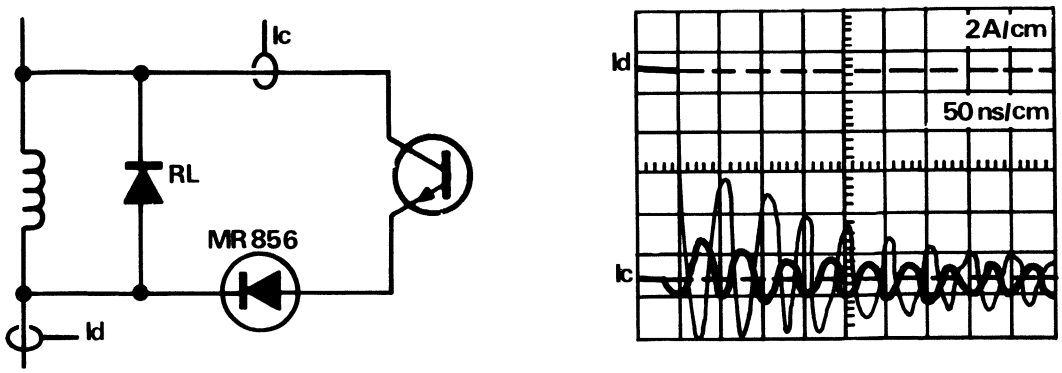


Figure 2-23

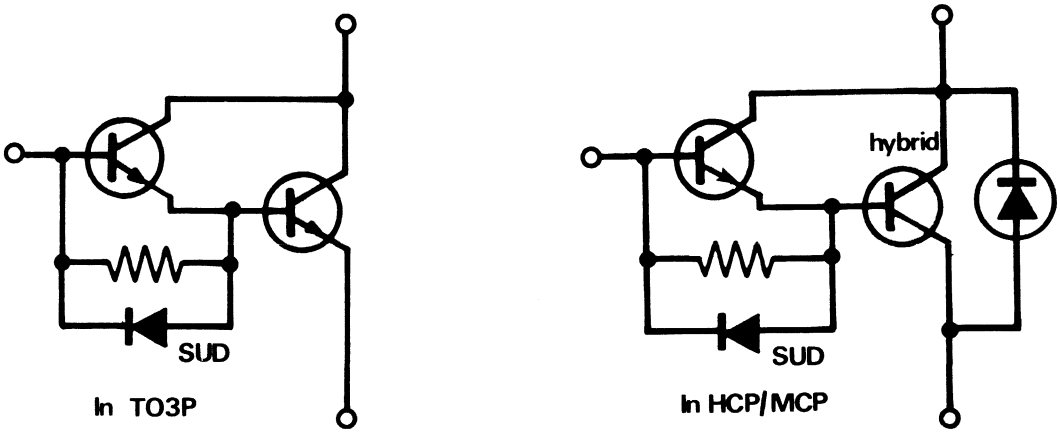


Figure 2-24

B) Switchmode III

B-1. Technology

B-1.1. IMPROVEMENT OF REVERSE BIAS SAFE OPERATING AREA (RBSOA)

When we studied the safe operating for bipolar transistors we saw that at turn off there was a high density of current at the center of the emitter finger.

This density can be high enough to create an avalanche injection and a destructive condition (RBSOA).

If this high current density could be reduced, then the safe operating area at turn-off would be improved.

Until now, the solution was to increase the depth of the base, but the turn off times being inversely proportional to this, increased significantly.

It seems evident that if we are near the limit of the safe operating area for as short a time as possible, we can increase the reliability of the device.

The reliability can be further increase by reducing turn on losses and thus reducing junction temperature.

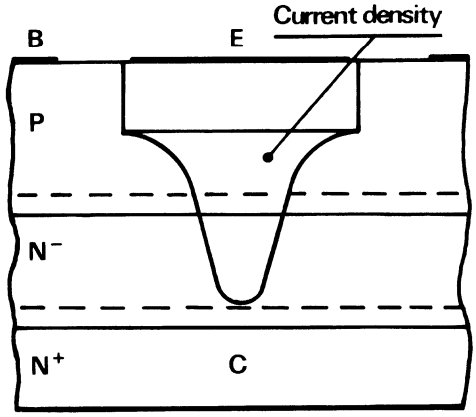


Figure 2-25

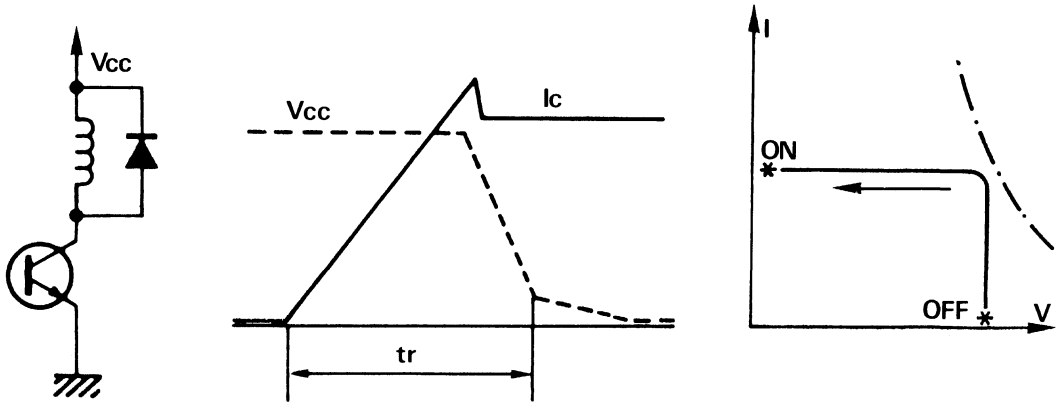


Figure 2-26

The devices used in these applications must be fast but at the same time have good safe operating area to assure good overall reliability. The question is: is this possible for a single device? Let's first look at what effect the geometry of the emitter has on the safe operating area under reverse biased conditions RBSOA.

If we wish to decrease the lateral field which pinches the current, the resistivity of the base must be decreased underneath the emitter fingers, however the peak gain is inversely proportional to this resistivity which introduces a compromise in performance.

The second solution consists in reducing the size of the emitter finger. However, if the length-width ratio of the emitter becomes too low, transitory localised debiasing

problems may arise, which may can cause reliability problems and lower peak gain. In fact, the injected emitter current is exponentially proportional to the emitter-base voltage (IE = k exp VB), and for slight variations in VBE there is substantial variation in I_E Here too, there is an optimisation of emitter geometry.
A third solution would be to place a single base only next to an emitter finger.

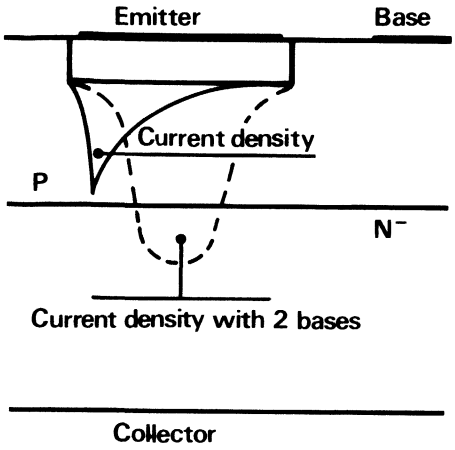


Figure 2-27

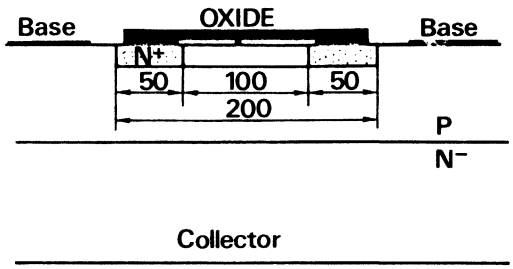


Figure 2-28

By using this variation the current density below the emitter finger is divided in 2 at turn-off. But debiasing problems, at turn-on, would arise affecting reliability, losses and emitter efficiency.
The aim of SM III technology is to combine the advantages of the last 2 solutions:
- narrow emitter finger
- dividing the current density under the emitter finger by 2.

We get, for example, the product below figure 2-28.

The emitter finger is divided into 3 sections, the center area, protected by an oxide, avoids diffusion of the N+ emitter and the emitter-base parasitic contact with the emitter-collector parasitic diode.

We now have 2 narrow emitter fingers (50 microns), each biased by an adjacent base to get a factor of 2 decrease in current density at turn off and an increase in RBSOA capability. Thanks to its small width, there are few debiasing problems thus not loss in peak gain.

The turn on characteristics remain very good because the current density increases during turn-on take place at the periphery, which hasn't charged.

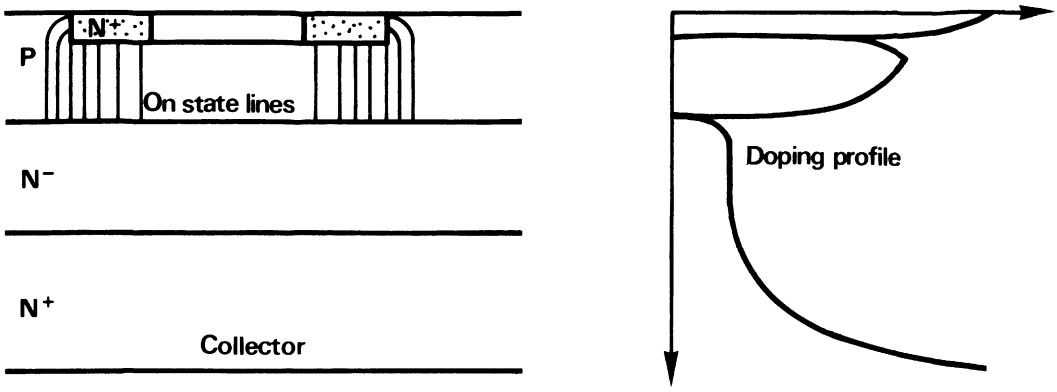


Figure 2-29

B-1.2. SPEED IMPROVEMENT

We have seen what needs to be done to improve RBSOA. We also know how important it is to have fast devices to improve reliability. How can these 2 parameters be combined in the same device? In the past when switching times needed to be decreased, it was necessary to introduce recombination centers or heavy metals: gold, platinum or to reduce the lifetime of minority carriers by gamma irradiation. At the same time, the base thicknesses were reduced and the peripheries of emitter fingers ZE were increased, but this often result in poor safe operating area capability.

For switchmode III technology, ZE is increased thus the ZE/area of the chip is increased, resulting in improved switching speeds. But the most important result was the almost complete reduction of deep minority carriers stored in N- region of the collector below the emitter finger area, which allowed significant improvement in speeding speeds, approximately 10 times the capability of standard technology.

B-2. Electrical parameters

B-2.1. SWITCHING TIMES

B-2.1.1. For turn on

In the "Darlington" chapter, we saw a table showing the maximum limits of the rate of current rise during turn-on which was governed by the technology of the device and that Switchmode III was significantly better then the classic bipolar: 500 A/microsecondes instead of 100 A/microsecondes, which results lower turn on losses.

B-2.1.2. At turn off

In the table below the various base drive conditions are compared for a switchmode III device.

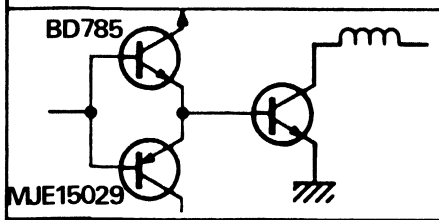
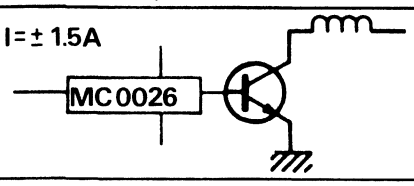
MJ16010 10A Ic/Ib=10		Tc = 25°C		Tc = 100°C	
	ns	Vbeoff-5V	⏚	Vbeoff-5V	⏚
	tc	30	150	50	200
	ts	400	1000	1000	4000
	tc	30	100		
	ts	1000	2000		

Table 2-2

We see that the switchmode 3 bipolar transistor has consistantly gives good crossover times, tc and since turn-off losses are proportional tc the turn-off losses are very low for this technology.

We also see that control without negative voltage could be sufficient for many applications.

B-2.1.3. Removal speed of dIb/dt

The speed of removal of carriers stored in the base and in the N- region of the triple diffused, high voltage transistors or standard technology, is usually limited to 4 or 5 A/μs to avoid premature turn-off of the base emitter junction and an "in situ" recombination of the remaining carriers.

For switchmode III, due to better emitter efficiency, and few carriers stored in the N-region of the collector dIb2/dt can be as high as 20 A/μs.

This stiff control during turn-off allows very fast switching times to be obtained, thus small losses at turn-off. With the proper base drive design switchmode III devices could operated efficiently all the way up to 100 kHz applications.

See figure 2-30 the different turn off oscillograms.

B-3. The future of this technology

With discrete products, peak gains are not very high but there is the possibility of eliminating this disadvantage by developing a Darlington with switchmode III technology. Work on this aspect of switchmode III device is continuing at Motorola at the present time.

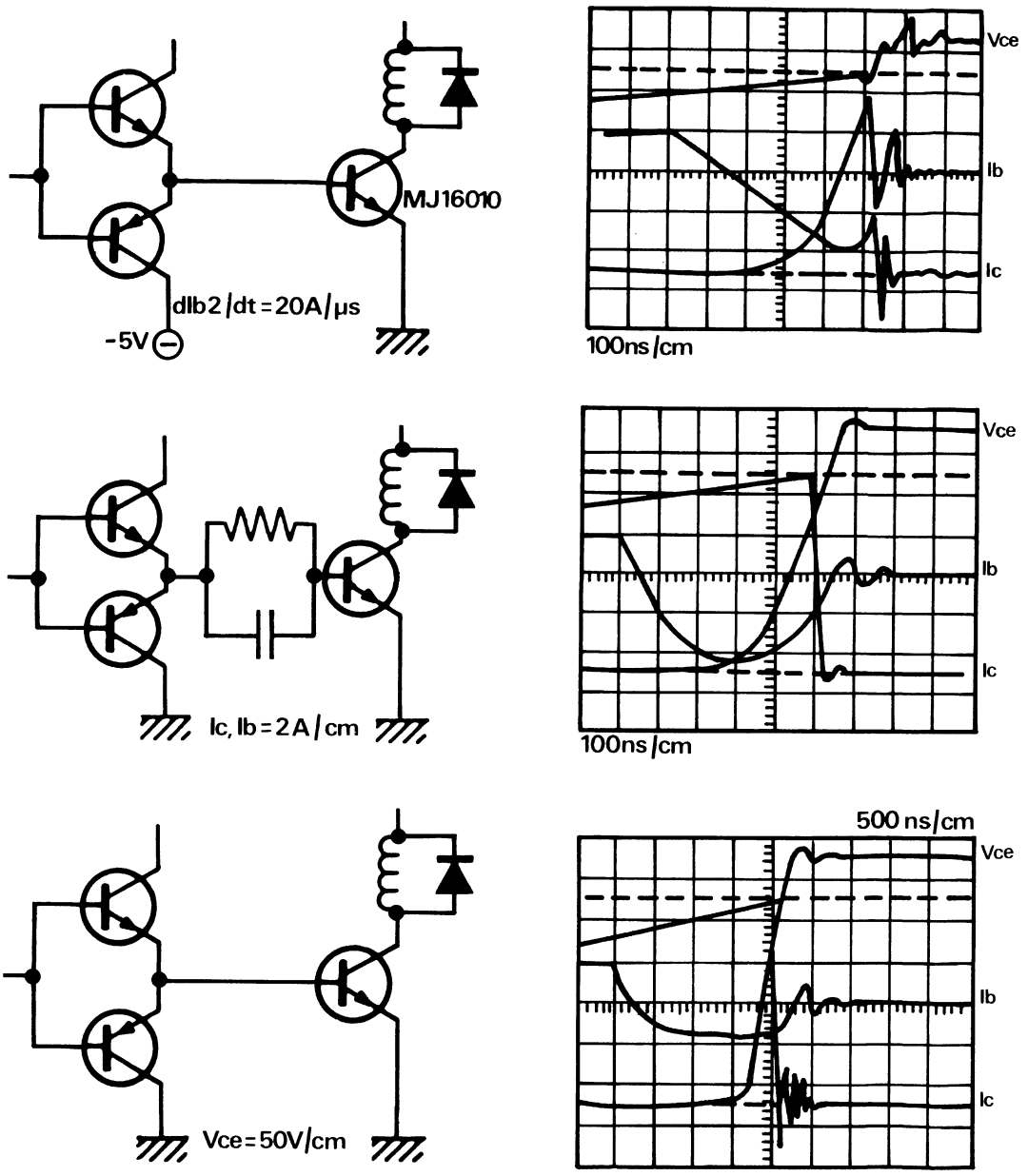

MJ16010
dIb2/dt = 20A/µs
-5V
Vce
Ib
Ic
100ns/cm
Ic, Ib = 2A/cm
Vce
Ib
Ic
100ns/cm
Vce = 50V/cm
500 ns/cm
Vce
Ib
Ic

Figure 2-30

2. Power MOSfet

A) History

The planar technology presented by Mrs. Khang and Atalla in June 1960 resulted in a reliable MOS structure (Metal Oxyde Semiconductor).

This technology immediately gave rise to the production of:

- integrated circuits
- amplification circuits with high input impedance
- high frequency amplification circuits

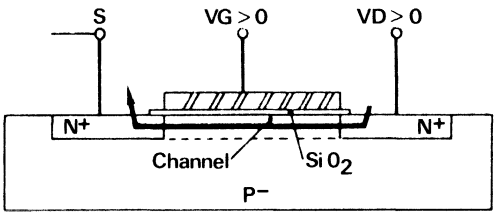


Figure 2-37 – Conventional MOS structure

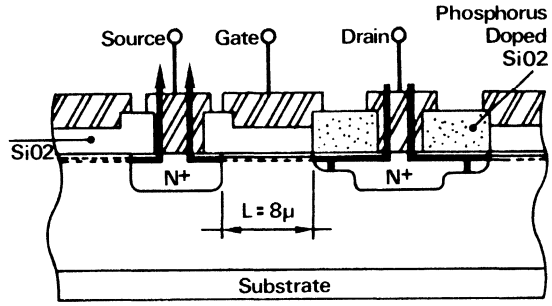


Figure 2-32 – 1968 Dawson structure

These initials MOS structures were not capable of supporting the two basic power device requirements:

- to be able to sustain high voltage
- conduction of high currents

These structures had potential qualities that where desirable in power transistors:

- negative $\Delta ID/\Delta T$ at high current,
- no storage effect of minority carriers, thus very short switching times
- input impedance greater than that of bipolars
- less intermodulation distorsion at high frequency than that of the bipolars (similar to that of pentodes)
- voltage control permitting high power gain

Different research groups tried to create structures capable of handling higher power.

In 1968, DAWSON created the first high frequency power MOS in the laboratory.

The characteristics of this MOS were 2 A, 100 V, 5 W up to 10 MHz, with chip area of 3 mm².

In spite of this, it wasn't until 1975 that power MOS devices appeared in the market having characteristics similar to Dawson's original model.

B) Main factors pf power limitation

The growth of the MOS structures into the power area was originally limited due to physical and geometrical constraints:

- breakdown of drain diode
- punch through of drain-source
- permitted current density

B-1. Breakdown of drain diode

The gate drive, the thickness of oxide layer, the area of the drain diode and width of channel, are the factors of the breakdown phenomenon.

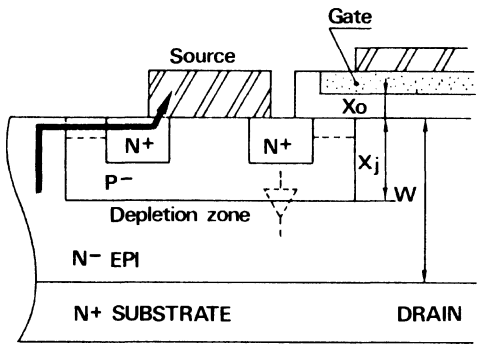


Figure 2-33 – Drain diode

In certain geometries, the presence of a metal gate near the channel provokes a concentration of field at the surface of the drain diode: this field causes a noticeable reduction of breakdown voltage. Suppliers of power MOS devices attempt to minimize the effect of this gate on breakdown voltage.

B-2. Punch through source drain

When the space charge region associated with the diode drain widens, and when it rejoins the source, punch through takes places and we have:

$$V_{PT} = L^2 \frac{qNA}{2\xi_0 \epsilon Si} \simeq K L^2 \ NA$$

L = lengh of channel, NA = region P doping.

To improve on this, structures were created with low doping in the N- drain region in order to allow the electric fiels to develop in this "drift" region.

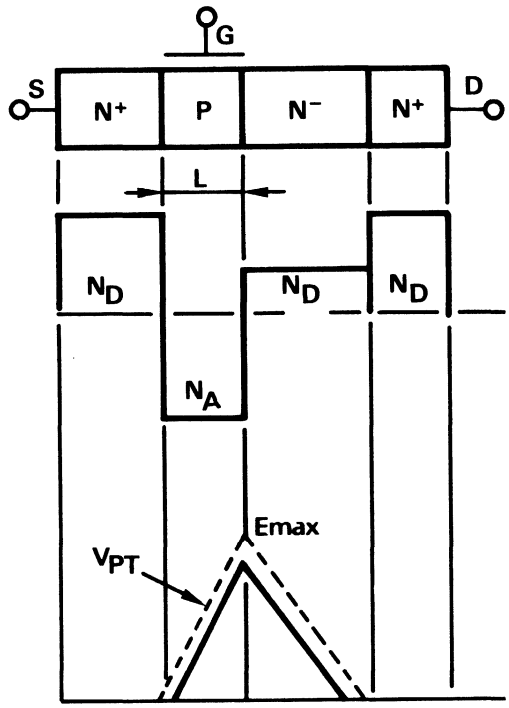


Figure 2-34 – Punch through of source drain

B-3. Permitted density of current

We have ID = μ effective COX Z/L f (Vg, VD, VT) we see immediately that drain current ID is a fairly complex function of both biasing and geometry:

COX: oxide capacity per unity of area, Z: width of drain, L: length of drain, μeff being the effective mobility of carriers.

The task for the designers, then is to find structures which increase Z, reduce L and increase COX at the same time staying within the limits of the technological constraints of:

- Lithography precision
- diffusion precision
- of breakdown VGD by COX

We shall now look at how the designers approach this complex technology of power MOS.

C) Power MOS technology

Modern power MOS can be divided into three families:

- structures with horizontal channel and uniform doping
- structures with diffused horizontal channel DMOS
- structures with vertical channel VMOS

C-1. Structures with horizontal channel and uniform doping

C-1.1. COPLANAR ELECTRODES

C-1.1.1. We have already seen the Dawson model which gave for an area of 3 mm², 2A × 100 V, only in N channel. Breakdown voltage may be increased by Si02 insulations, phosphor-doped, stopping the gate from approaching the drain region N+.

C-1.2. TRANSISTORS WITH FIELD PLATE recently (1976) Hitachi created a complementary pair of MOSfets with coplanar electrodes, uniform doping and implanted channel.

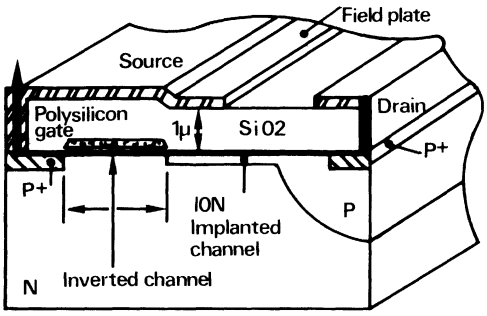


Figure 2-35 – Hitachi 1976

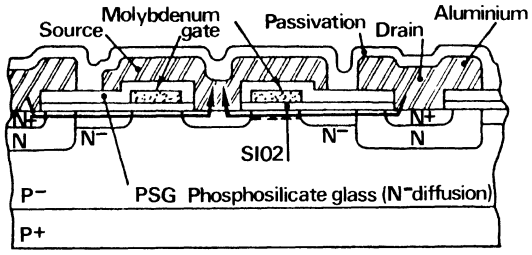


Figure 2-36 – Hitachi 80

The source electrode, situated above the silicon, reduces the amplitudes of the electric field in silicon area, and so increases voltage and current ratings at the same time.

OKABE thus obtained 10 A, 200 V, Rdson = 1.2 Ω on a 20 mm² chip.

This type of structure is mainly used for its linearity and complementary capability in Hifi amplifiers.

C-1.1.3. MOSfet with molybdenum gate

Once again, the source electrode acts as a field plate. The gate is produced in molybdenum, as this has an access resistance 50 times lower than polycrystalline silicon, thus enabling good switching times and operation at high frequency (1 KHz to 30 MHz).

HIROAKI thus developed 8 A, 100 V, Rdson = 1 Ω capability on a 20 mm² chip.

C-1.2. NON COPLANAR ELECTRODES

This configuration was chosen because it eliminates complex metallization on top of the chip.

C-1.2.1. Interdigitated structure

The first structure created in 1974 by MORITA was a P channel with the source at the base of the chip.

He thus obtained a MOSfet of 2.2 A 55V, capable of operating up to 1 GHZ, on a 1.4 mm² chip.

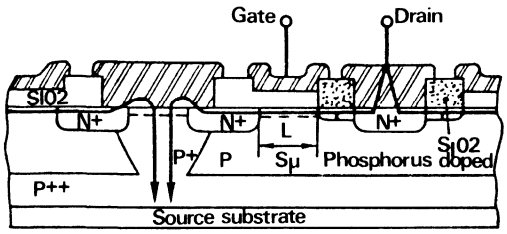


Figure 2-36 – Morita 74

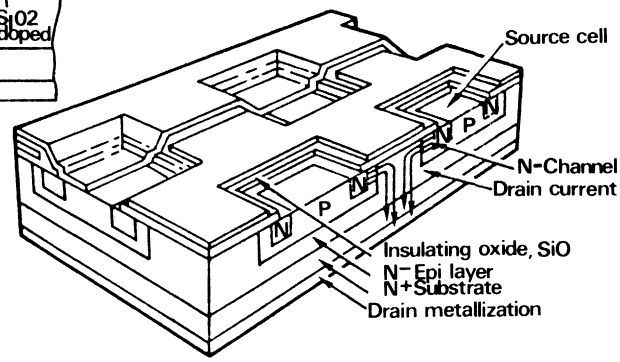


Figure 2-37 – TMOS stitched structure

C-1.2.2. Stitched structure

This is presently the most widely used structure it is the reverse of the preceding one: the drain is at the base of the chip.

The advantages of this type of structure are:

- having the gate above the low-doped drain region,
- having a source metallisation above the chip which acts as field plate.

This structure also allows a fairly simple diffusion process, without too much masking, the polysilicon gate serving as self-alignment of source windows, and results in the best Rdson/BVDSS compromise.

It has the disadvantage of having high interelectrode capacitance and non negligible gate resistance, which increases switching times and limits frequency of use.

The first to produce such a geometry in P channel was Yoshida for Hitachi in 1976. He obtained 20A, 85V, Rdson 0.5 Ω on a 25 mm² chip.

Next came International Rectifier with the hexfet in 1979 (hexagonal shaped sources), then Siemens 1979 created the SIPMOS with square-linked structure with double ionic implantation (P and N+ source).

Finally Motorola, also in 1979 introduced their TMOS power MOSfets.

C-2. Diffused horizontal canal DMOS

The only example of this structure is a Signetics product invented by Siggs in 1972. This structure is such that the gate is not above the drain N+ region and the N- region controls breakdown. The interdigitate structure is complex and does not allow for control of high currents 0.1 A 300 V, but can go up to 3 GHz.

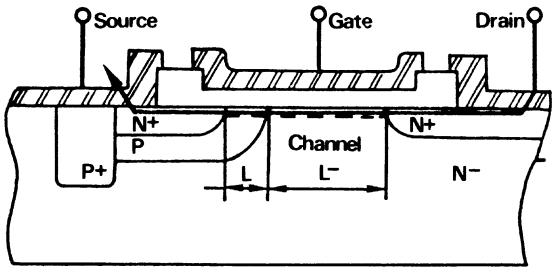


Figure 2-38 – DMOS

C-3. Vertical channel structures

Using the chemical erosion process of silicon, channels which are more or less vertical are created in the structure, they can be divided into 2 families.

C-3.1. ISOTROPE ETCH

This was produced in 1975 at Westinghouse by Heng. The structure has the following advantages:

- easy to obtain channels of slight length
- reduction of parasitic capacitance by suppression of source metallization above the gate

The main inconvenience is the complexity of production steps for the gate. On a 0.4 mm² chip he obtained: 2A 28V Rdson = 2 Ω, and this products can work up to 2 GHz.

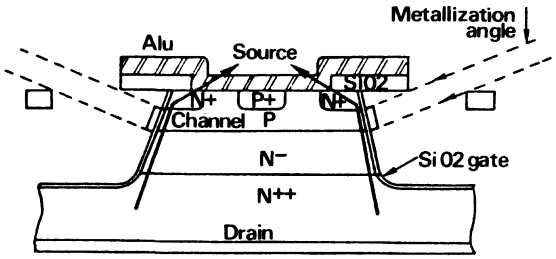


Figure 2-35 – Isotropic etch

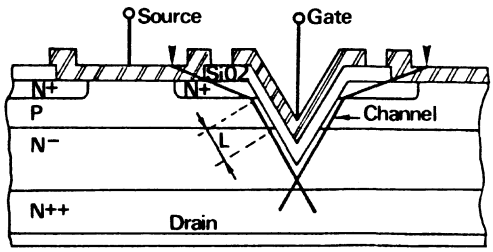


Figure 2-40 – Siliconix VMOS

C.3.2. ANISOTROPIC ETCH

The first highly commercialized power MOSfet, the interdigitate VMOS by siliconix in 1975. The V is obtained by chemical etching across the source. The advantages of this kind of structure are based on the simplicity of control of geometrical dimensions.

Each etching produces two channels which doubles current capability which is the same as reducing the usefull area of the chip.

The major disadvantage is strong electric field at the point of the V, this high electric field creates yield problem on high voltage product.

It has produced 2 A, 90 V, Rdson 2 Ω product on a 1.5 mm² chip, capable of giving out 30 W at 185 MHz.

This structure was improved in 1979 by Siliconix by a using a linked VMOS (Kay). He obtained 10 A, 400 V, 1 Ω on a 15 mm² chip.

To avoid the electric field at the botton of the etch, Salama in 1976 created a U-structure and obtained 1 A, 35 V, 4 Ω on a 0.25 mm² chip for 5 W at 800 MHz, but because of the coplanar structure the breakdown voltage was low.

Next came Temple of General Electric in 1979 and 1980 who created the flat based VMOS with Junction Termination Extension (JTE) to replace the diffused guard rings or field plates, thus enabling production of power MOSfets of 600 V and 6 Ω of Rdson.

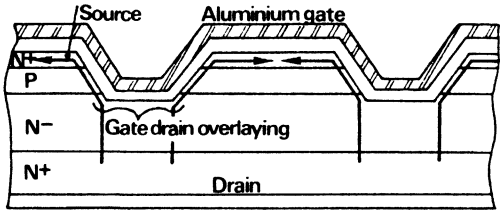


Figure 2-41 – VMOS with GE flat base

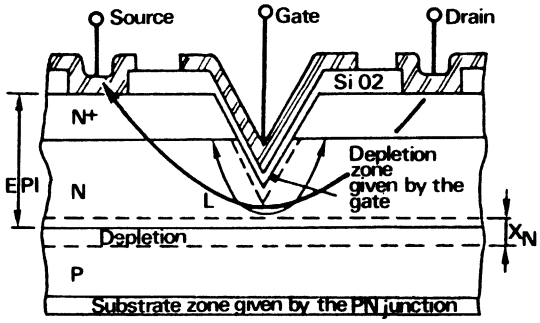


Figure 2-42 – Depletion VMOS

Finally, Siliconix in 1980, brought out the **Triplanar** (flat – based VMOS) allowing 5 A, 400 V and 1.4 Ω of Rdson to be obtained, we cannot leave aside the anisotropic etch vertical channel without mentioning the only depletion MOSfet, VMOS Farzan-Salama in 1975.

Contrary to all the other structures where the current circulates in a superficial inversion channel, here, it circulates in a volume modulated by the gate voltage. This device is very close to field effect transistors.

This structure by use of majority carriers is capable of higher currents, mobility of carriers being greater in volume than on the surface. This system can work by enhancement and depletion and its manufacture is simple.

Unfortunately the coplanar electrodes do not lend themselves to good density of integration and voltage rating is mediocre: 1.4 A 55 V 2 Ω, 12 W at 80 MHz with a 1.2 m² chip.

We have seen the different results obtained by the product designers during the last 10 years, now we shall look in detail at the choice they have had to deal with.

D) Technological choices

D-1. Choice of geometry of the source

We know that $I_D = \mu o\ Co\ Z/L\ F\ (V_D,...)$. Therefore ID is a function of the width of drain Z.

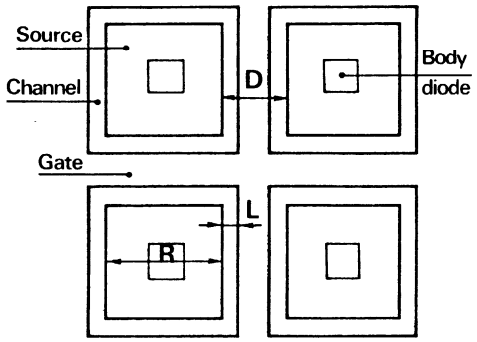


Figure 2-43 – Top view of a square linked structure

If we take a square geometry for each cell, we see (Figure 2-43) that the width of the channel is equal to the perimeter of source Z. to give maximum current. We can thus define a parametric relation by area units: Z/A which is a factor of quality. In order to integrate all the geometric variables, it is better to trace the relation without Z.D/A dimensions in function of a parameter linked to the cell reproduction step R/D which gives, for different geometries:

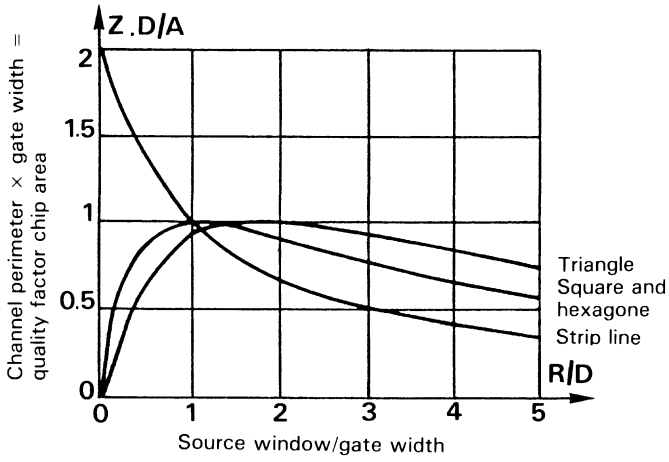


Figure 2-44

On these curves we see that the optimum quality factor is obtained for R/D = 1, that is to say when the gate width is identical to a side of the source.

On the other hand for low voltage MOS, it is important to increase density of integration, i.e. to increase the number of cells by area unit or to reduce L and d to maximum to give maximum current per area unit.

D-2. Choice of drain

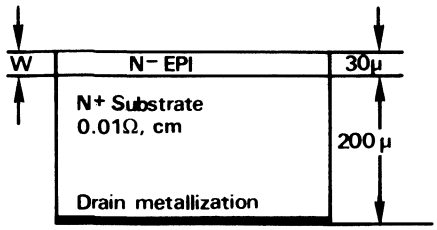


Figure 2-45 – Drain body

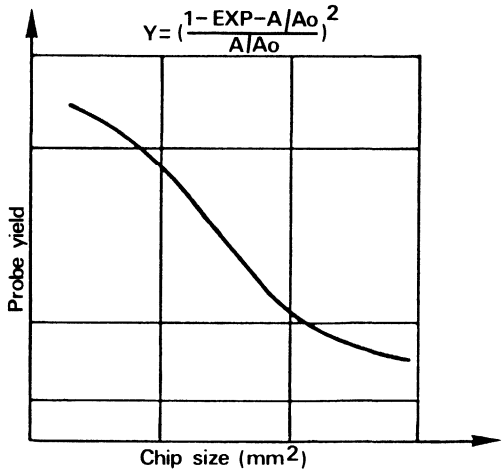


Figure 2-46 – Power MOSfet, die size/probe yield

The drain in the vertical current power MOS is the volume part of the silicon. This is composed of a slightly resistive substrate of silicon (series resistance) on which several tens of microns of silicon, lightly doped, have been grown in plan 100 by epitaxy. How is this epitaxied silicon chosen? We know that, roughly the breakdown voltage: $V_{BR} = K$ W/ND so far high voltage products a thick epitaxied zone must be chosen:

W large is low-doped: ND low. But a compromise must be found, as Rdson = $8{,}3 \times 10^{-7}$ $VBR^{2,5}$ A^{-1} with A in mm^2 so with high BV we have a high Rdson, leaving the possibility of increasing A but one is soon limited by production yields which have the form:

$$Y = \left(\frac{1-\exp -A/AO}{A/AO}\right)2$$

A: chip area – AO: known chip area of known yield.

When A increases the yields diminish significantly, and so costs increase proportionately. The VBR nearest the maximum voltage should be chosen to get the smallest possible Rdson. The greatest possible A should also be chosen compatible with production yields and it is always better to place the chips in parallel in the same package for this situation: CMOS = K A/XO.

D-3. Choice of P Well (channel)

The choice of doping for P Well: NA and the length of drain are given by punch-through voltage. $\boxed{VPT = \alpha L^2 NA}$ we notice immediately that there is a compromise to be made with the maximum MOSfet current. $IDmax = \beta/L$ L minimum for IDmax maximum and L maximum for VPT maximum, for older power MOSs: $L \cong 10\mu m$ but for more recent structures: $1 < L < 5\mu m$ the question of level of threshold voltage of the power MOS

also enters in the choice of P well, as $V_{TH} \cong F(\sqrt{N_A})$ for good noise immunity and dV/dt it is essential to avoid a Vth which is high enough but not too high, so that control is relatively compatible with the supply voltage of existing logics. In modern power MOSs VTH is between 3 and 4 V.

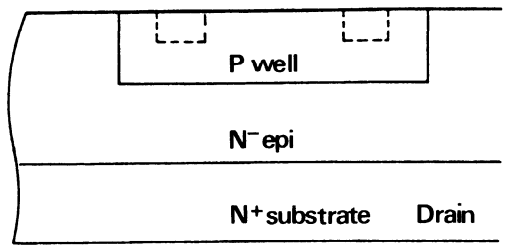


Figure 2-47 – P Well

D-4. Choice of gate

The gate must have the following properties:

- low access resistance
- low leakage current
- good time stability
- high breakdown voltage
- low input capacitance
- simple technology

The first gates were made in aluminium, this kind of material having practically all the desired qualities except that aluminium contains sodium which has a certain tendancy to move into the silicon dioxide creating stability and reliability problems. Another possibility is for the gate is to use molybdenum which has all the qualities except for cost.

The answer was to work on the silicons:

- monocrystalline silicon, far too resistive and expensive
- polycrystalline silicon, less resistive than monocrystalline but 3000 times more resistive than aluminium and 50 times more than molybdenum. This resistance does not however impede the speed of present power MOS as: internal RC ≅ 1ns. Its advantages are that it can be N+ doped at the same time as the source, so its qualities can be controlled.

D-5. Choice of source

We have already looked at the influence of the source geometry.

Diffusion or ionic implantation of the N+ source serves to control precisely the length of the inversion channel and its doping is high to reduce access resistance.

It is also necessary to have a device allowing easy paralleling of elementary cells, and thus of non-coplanar electrodes.

The best source device is one which permits complete metallization and thus better temperature distribution.

D-6. Manufacturing stages for the N type TMOS

In the following Figure 2-48, we can see that to manufacture a power MOSfet, one must start with a monocrystalline silicon plate of type N+ on which several tens of N- microns (depending on desired breakdown voltage) have been grown using an epitaxial process.

Next, in a series of 6 masks, the succeeding operations insulate the gate, increase the gate in polycrystalline silicon, create P channel, N+ source, insulate the gate and globally metallize the source.

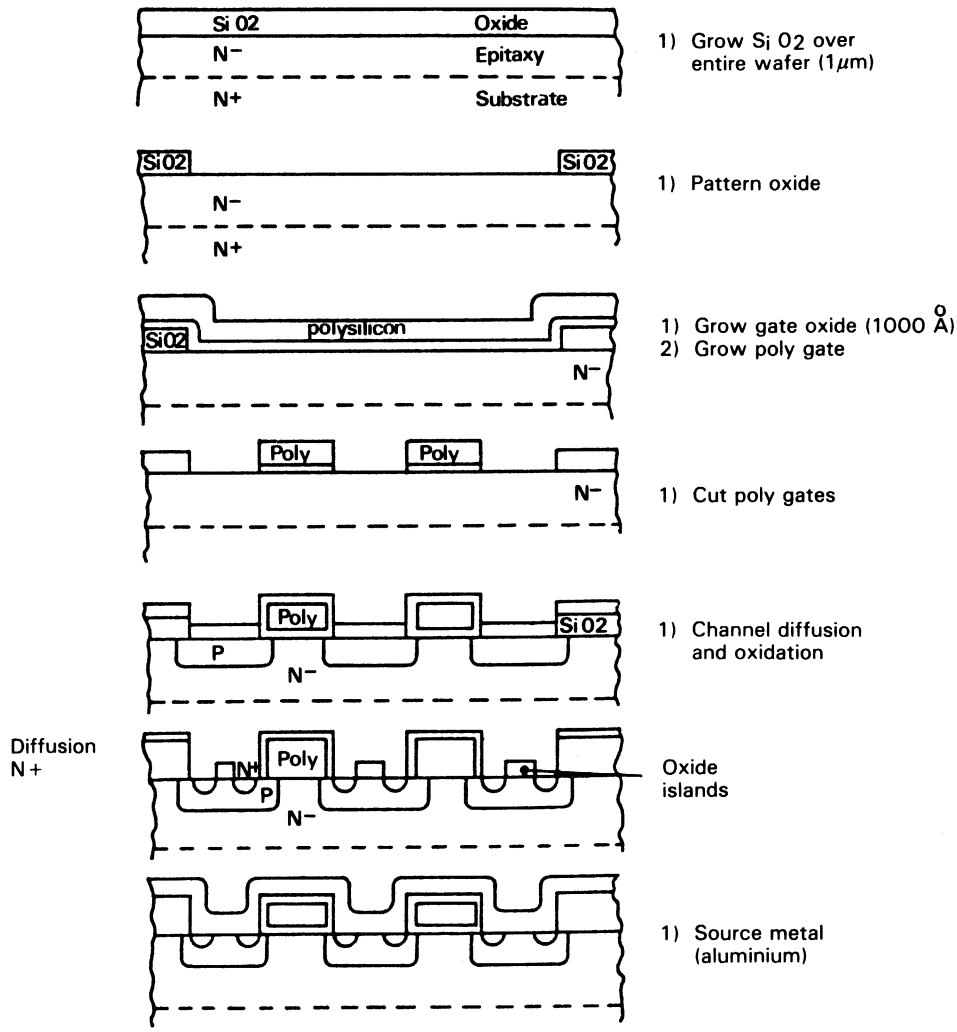


Figure 2-48 – TMOS process steps

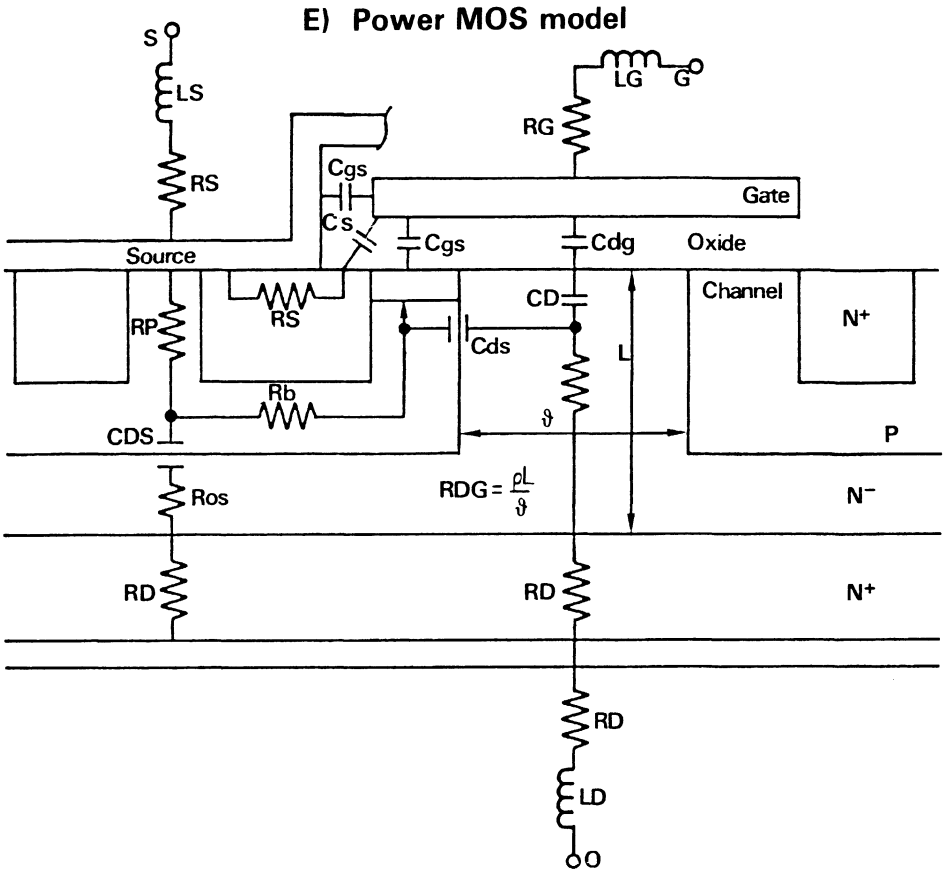
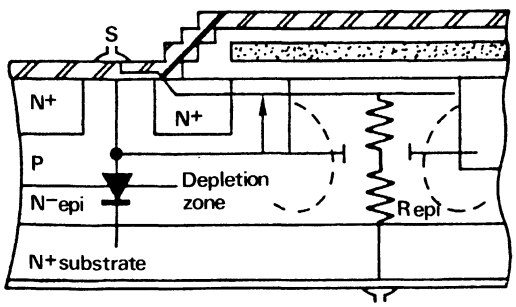


Figure 2-49 – Complete model of TMOS

From this angle with all the TMOS parasitic impedances, or, to generalize, all horizontal channel MOSs, linked structure and vertical current, we can, by simplifying, deduce several models.

E-1. A model demonstrating operation



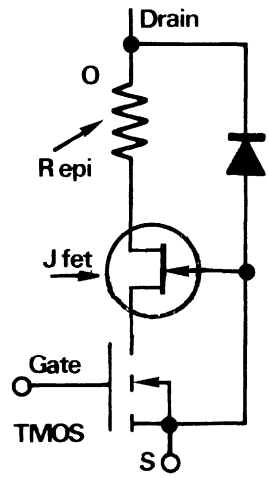


Figure 2-50 – Equivalent diagram, LF model of TMOS

In fact in this model, we see first of all, the classic power MOS structure with modulated gate, source and drain.

The PN parasitic diode, gives a depletion region which accentuates with bias and so more or less pinches off the N- region of the drain (drift zone): so we have a pinched JFET of channel. This very low doped drift zone is resistive, we obtain that series resistance which is the greatest part of the Rdson in medium and high voltage MOSs. The diode drain is in anti parallel to all this.

E-2. The power MOS may be shown as either of the following figure.

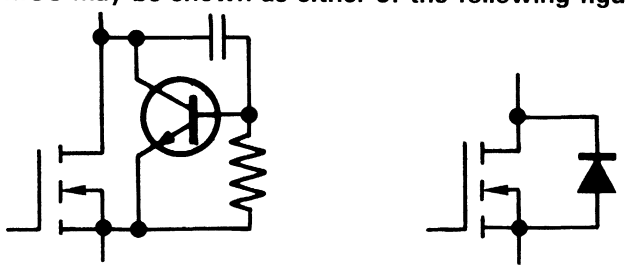


Figure 2-51 – Symbolic representations of power MOS

Diagram a) shows the MOS plus the NPN parasitic transistor (source – channel – drain) with the source and channel connected by a low value resistance (P zone resistance), for low frequency and switching models, this resistance can be considered to be zero, so we see only the collector base diode (diagram b). In any case for fast transistors, or fairly high frequencies, this resistance is no longer negligeable and we have a transistor in parallel with the MOS which may give rise to certain faults (breakdown, voltage, etc.).

E-3. For fairly high frequencies the power MOS may be shown as in the figure below.

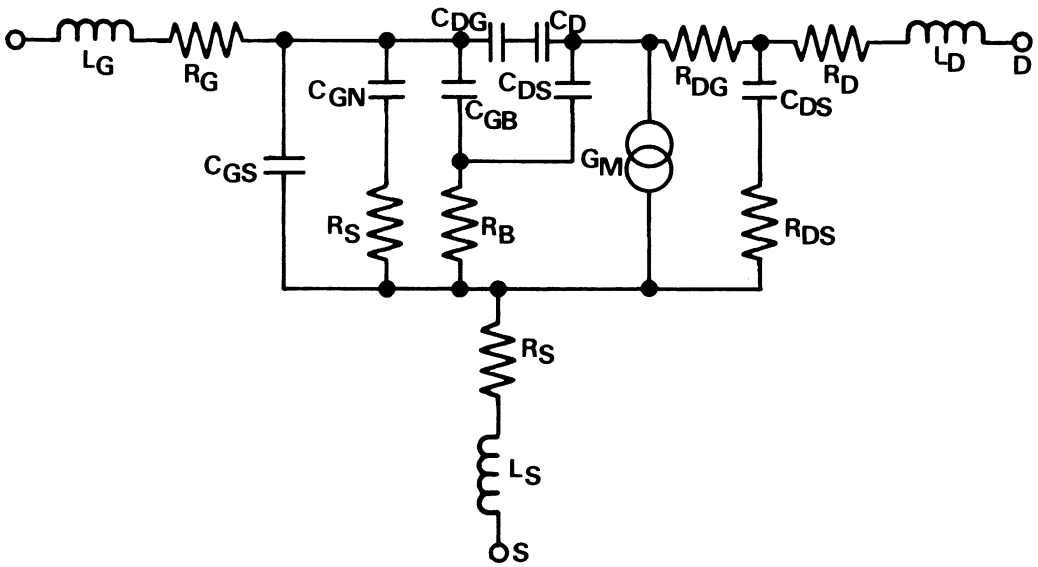


Figure 2-52 – Modelling of TMOS

This model is not very practical for most applications (other than computer modelling), it can be further simplified, giving

E-4. Practical model of TMOS

Resistances and reatances of access have been left out. CGS and CDS depend only on the products geometry. CD is a dynamic capacity which depends on load variation in the N- drain. RDG in the resistance in the low doped N- region of the drain. CDS and RDS are due to the reverse diode, so CDS varies in K $VD^{-1/2}$ as on a diode.

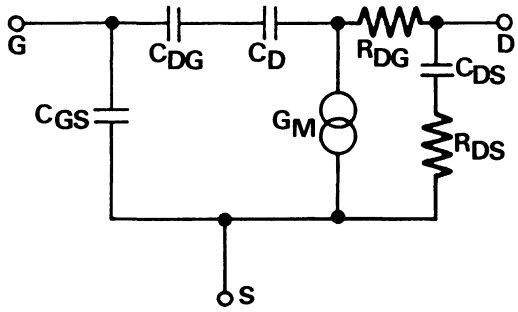


Figure 2-53

F) Output admittance of the TMOS

This output admittance (Y22) changes sign for a critical value of load current: critical I.

We have Imax for the same frequency which ID varies.

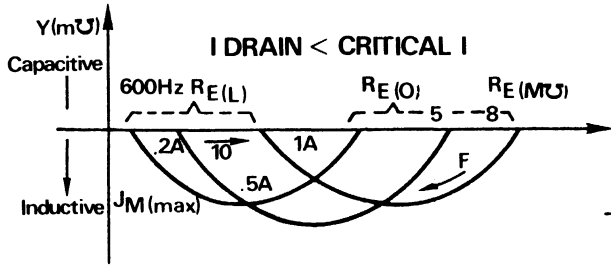


Figure 2-54 – Output admittance

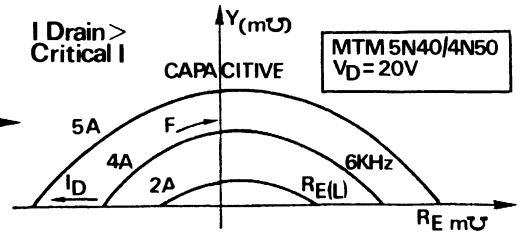


Figure 2-55 – Output admittance

Using these curves, we can show variations in real and imaginary parts, at O frequency and L frequency and ID function.

We get:

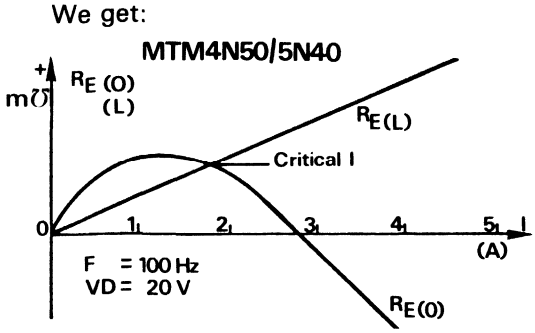


Figure 2-56 – Variation of Y22

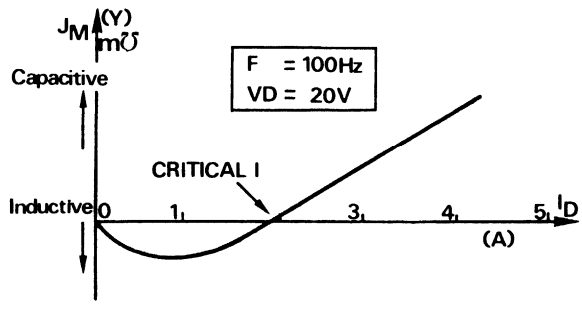


Figure 2-57 – Variation of this admittance as a function of frequency (Bode plan)

We can summarise these variations with the following output diagram of power MOS.

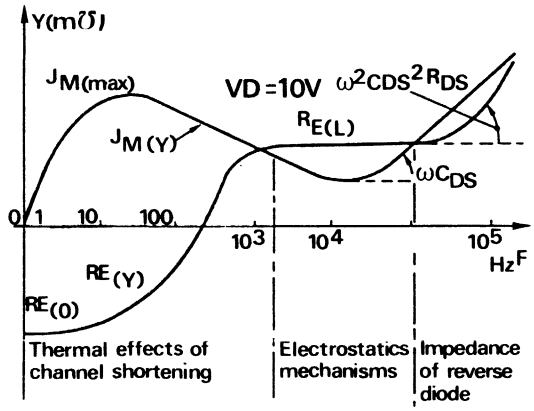


Figure 2-58 – MTMSN40/4N50

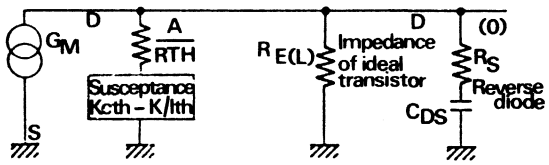


Figure 2-59

For low frequency (<100 KHz) the output admittance is due to thermal effects and channel shortening. For high frequency (>100 KHz – 1 MHz) the real part remains constant, only the electrostatic mechanism due to the drain imposes resistance. For very high frequency, it is the parasitic impedance of the diode which gains the upper hand imaginary $J\omega$ Cds and ω^2 Rds in real part.

G) Main characteristics of power MOSfets

G-1. The Rdson – VBR compromise

G-1.1. COMPONENTS OF Rdson RESISTANCE

From the curve in Figure 2-60, Rdson F(Vg) we see that for the type of structure we are studying Rdson resistance saturates after a certain value Vgate (VG) higher than 8-10 V. It is this value which we shall call RON ∞ which interests us. This resistance can be broken down into 3 resistance (Figure 2-61). The channel resistance which develops below the gate: Rch – Ra resistance of silicon access in N- region below the

gate: a layer which forms when VD<VG.RON ∞ = Rch + Ra + Rd. Rd resistance of epitaxial N- region contained between the access resistance and N+ substrate.

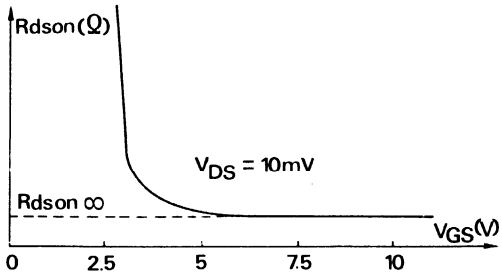


Figure 2-60 – Rdson versus VGS

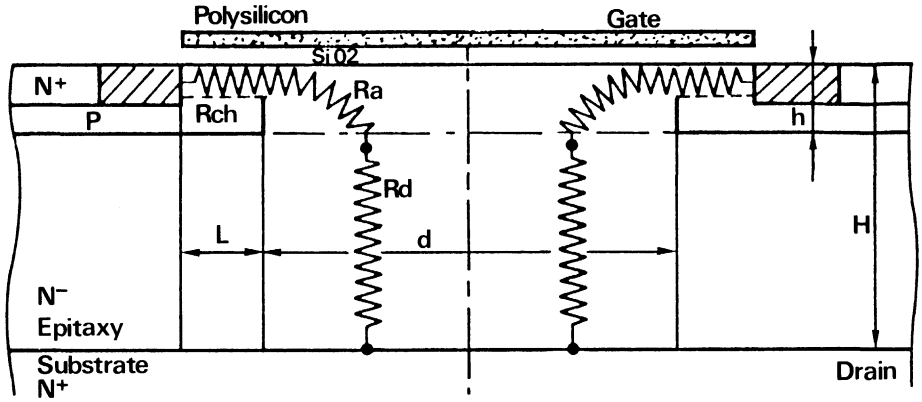


Figure 2-61 – Rdson components

G-1.2. Rch CHANNEL RESISTANCE

A simplifying hypotheses:

- doping in the source drain direction is constant
- heating of the channel due to the dispersed power is not considered
- the shortening mechanism of the channel due to electrostatic action of the drain voltage when the transistor operates in the saturation state is omitted, and the definition of the channel resistance: Rch = VD/ID when VD tends towards 0, we get:

$$Rch = \alpha \frac{L}{Z}\left[\frac{V'G+\Psi-2\phi F}{VG-VT}\right] \quad (1)$$

α being a constant depending on the physical characteristics of the materials used (carrier mobility, oxide capacities...) VG being gate drive and V'G effective gate drive, Ψ a potential translating parasitic effects ϕF Fermi potential of P semiconductor VT threshold voltage.

From this formula, we see that for a given family of semiconductors the channel resistance is defined exclusively by geometric factors:

- Z = sum of perimeters of all parallel channels
- L = channel length

G-1.3. ACCESS RESISTANCE Ra

This resistance is the composite resistance contained between 2 cells of a MOS of height h and width d (see Figure 2-61). It is linked to two mechanisms, the presence of the accumulated charge induced by the gate in the N- region the resistivity of the N- material, the formulation of this resistance becomes:

$$Ra = \frac{2h}{Zd}\,\frac{1}{\rho}\,.\lambda \qquad (2)$$

so the resistance of a silicon bar of section Zd/2 of length h and resistivity ρ (or with proportionality doping coefficient ND) multiplied by a factor depending on geometrical dimensions, of doping and VC. λ is always higher than the unit, its variation may be traced according to intercellular distance d, of doping ND and the depth of diffusion of P channels: h, VG being fixed at 15 V and the oxide thickness on the gate = x0 = 1000 Å (see Figure 2-62). The asymptotic limit of λ when d > 10 μm may be written as:

$$\lambda = \frac{d}{2}\sqrt{K\,\frac{ND}{h_2 F(VG)}}$$

we see on this curve, that λ is high for low voltage products (ND high and h low and becomes negligeable ($\lambda \# 1$) when ND becomes low (10^{20}) and d becomes high: results in a high voltage device.

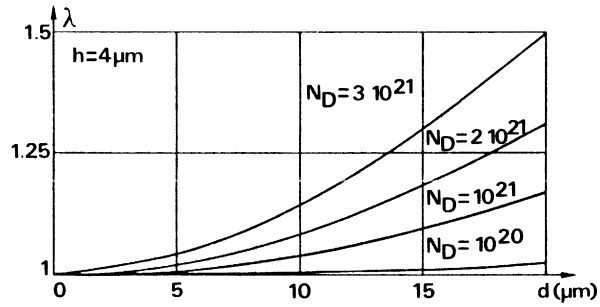


Figure 2-62 – λ = F(d) | ND,h

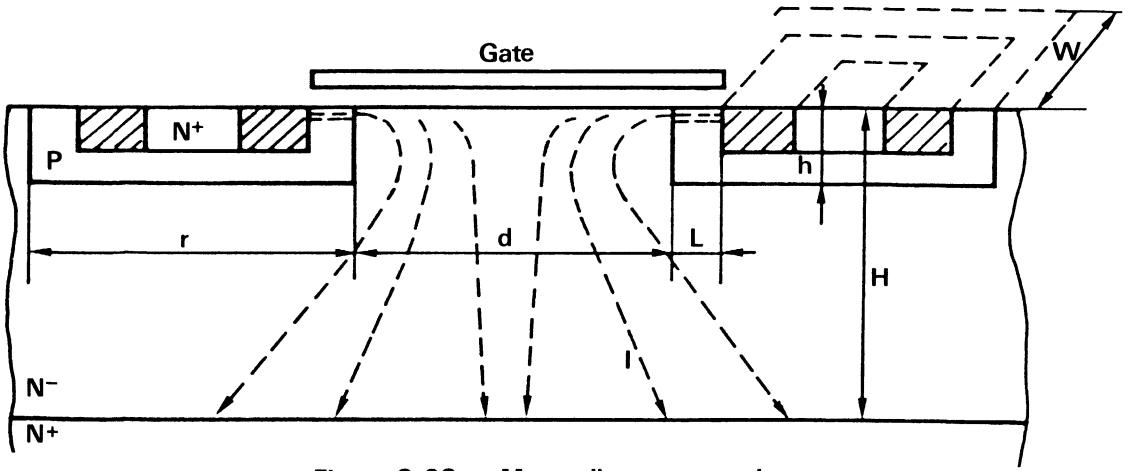


Figure 2-63 – Mos cell, current paths

G-1.4. DRIFT ZONE N- RESISTANCE = RD

The resistance of this epitaxial region with low doping is in the form:

$$Rd = \Gamma \frac{\rho}{W} \left(\frac{H-h}{d+r}\right) \quad (3)$$

Term $\frac{\rho}{W} \left(\frac{H-h}{d+r}\right)$

is the resistance of a silicon bar of section W(d + r) and length (H − h) = Rd (volume) (see Figure 2-63).

Coefficient Γ translates the spreading effect of the current caused by geometric dimensions H, h, d and r, this spreading arising when (H − h) > d/2 which is the case with high voltage MOSs. When (H − h) < d/2 as in the case of low voltage MOSs, there is no spreading and we may write:

$$Rd = \frac{\rho}{W} \left(\frac{H-h}{d}\right)$$

so that by introducing resistance volume Rdv as defined before, we always have

$Rd = \Gamma$ Rd volume (4)

and here: $\Gamma \Big|_{(H-h) \ll \frac{d}{2}} \simeq 1 + \frac{r}{d}$

If we draw the variation of Γ = Rd/Rdv as a function of d/H − h we obtain the curves in Figure 2-164.

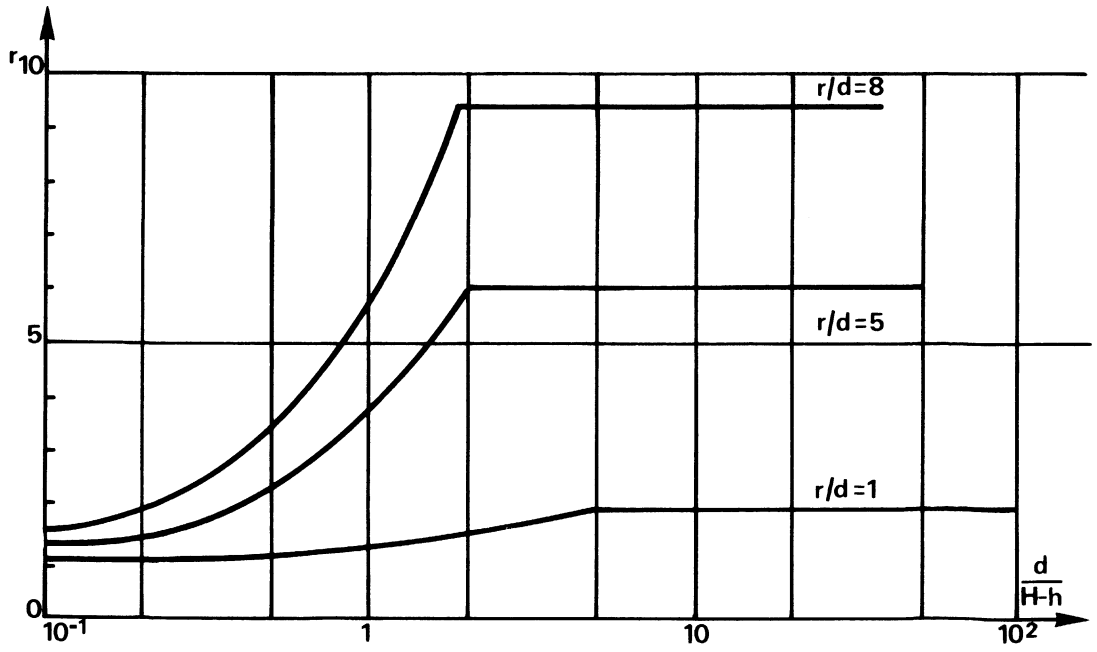


Figure 2-64 – Asymptotic function of defocalisation versus geometrical factors

G-1.5. VOLTAGE RATING OF VGs MAX OXIDE LAYER

If the gate is never open, there is a shield effect caused by the presence of the P+ N- diode and its bias of VDS voltage.

Calculation of the oxide thickness only takes account of maximum voltage, gate – source would be around 50 V for 1000 Å. So the VDMOS structure, by its geometric configuration could work under very strong drain source voltage even with a slight oxide thickness, (usually 1000 Å). The horizontal planar MOSs do not have this shield effect.

G-1.6. VOLTAGE RATING OF VDS MAX DRAIN SOURCE

A VDMOS structure at blocking may be seen like a P+ N- N+ diode. The breakdown is considered as happening frontally, that is to say that the junction curvature effects are overlooked (Figure 2-65).

In writing out the equations of the electric field and the optimisation of this to get minimum resistance in the on state (once the depleted space charge has invaded all of N- region) we get a pair of values ND and H – h as a function of VBR, which optimises Rdson (Figure 2-66).

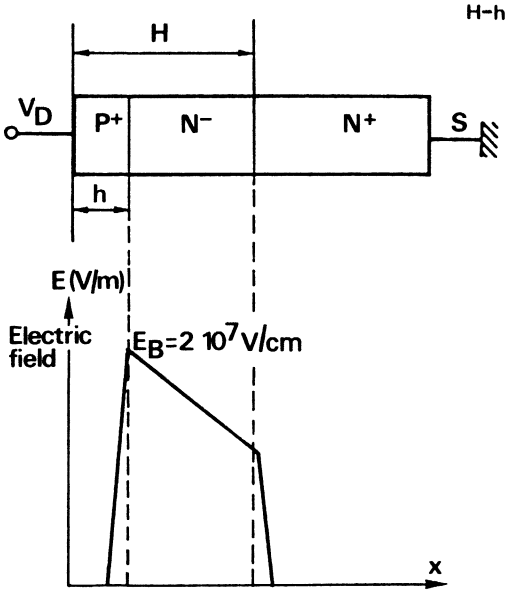


Figure 2-65 – Breakdown voltage in MOS structure

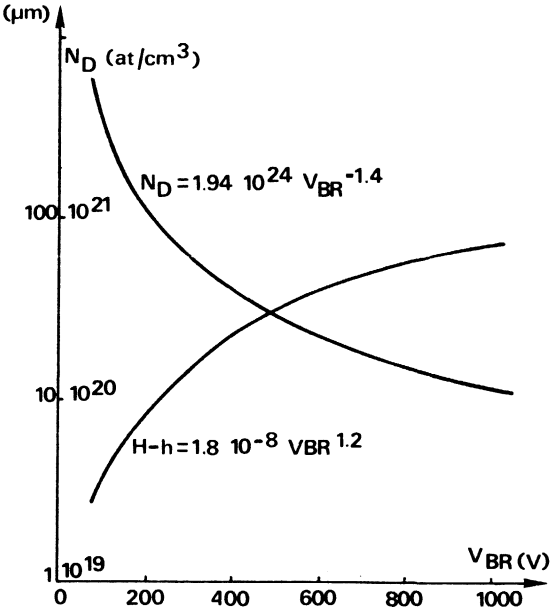


Figure 2-66 – Depth of epitaxial layer and doping level of this versus VBR for minimum Rdson

G-1.7. EXPRESSIONS OF Rdson

We have RON ∞ = Rch + Ra + Rd, i.e.

$$RON \propto \alpha L/Z + \beta (h/Z.d)\, \lambda VBR^{1,3} + \delta (1/S)\ VBR^{2,5} \qquad (5)$$

G-1.7.1. Low tension structure (<100 V)

For this type of structure, because of the practical limitations of precision lithography and masks, we are far from the electric fields (E = V/ L) junction limits in the silicon, so

only the first term of the equation (1) is predominant and can be verified with real VBR values, L and d, knowing that today, with the most up to date techniques of double diffusion, the length of channel L is about 0, 6 to 1 μm and the minimum distance between cells is around 10 μm, so the Rdson by unit area of a low voltage structure is only in fact limited by the integration density. If this integration density is optimised (r/d$\cong$1 for example for the TMOS) we can also write this an: RdSon = α Ld/S with α = 1/34 if L and d are in μm and S in mm^2.

G-1.7.2. Medium voltage structures (100 – 400 V)

The weights of the 3 terms in equation (5) become more or less identical, so the optimization of integration density seen in the chapter before, comes into play here.

The second phase of optimization should be analyzed for λ (i.e. λ tends towards 1). Strictly speaking this optimisation occurs when d (distance between cells) tends towards 0, but we must admit that for structures included within 100 and 400 V this condition is satisfied when d is less than 10 μm.

G-1.7.3. High voltage structures (> 400 V)

Geometric considerations are less and less important except that electric fields limits are now taken into consideration, so the 3rd term of the equation . (5) So we have: RdSon = $\delta \frac{\Gamma}{S} (VBR)^{2,5} = 8,3\ 10^{-7} \frac{\Gamma}{S} (VBR)^{2,5}$ with S in mm^2.

The lower limit (asymptote) of this equation is given for $\Gamma = 1$. This theoretical limit may be strongly increased if doping specifications (and geometrical accuracy sizes) are not respected, for example $\Gamma = 2$ if we have a doping inaccuracy of factor 2 (10^{20} in relation to 2.10^{20} for example).

This demonstrates the precision of reproductibility which must be obtained in epitaxial increase and in doping thus the "technicality" necessary for optimised VDMOS structures (Figure 38).

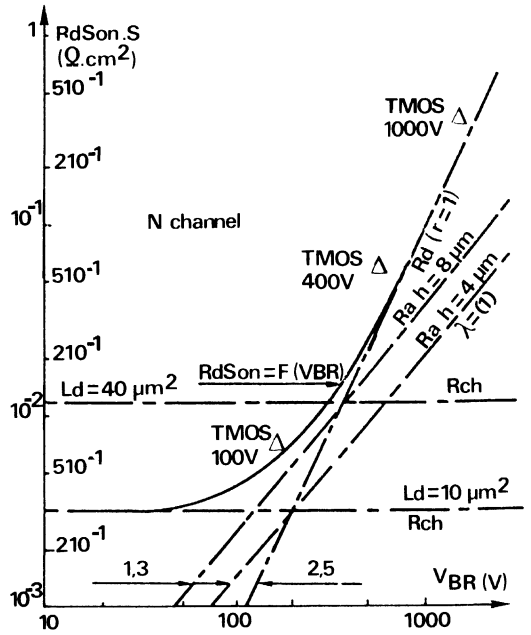


Figure 2-67 – Rdson = F(VBR) (asymptotes)

G-1.8. CONCLUSIONS

G-1.8.1. On the graph in Figure 2-67, we see that the Rdson limit for all channel N VDMOS structures is the line with a slope of 2.5 in logarithmic coordinates: this limit is created by the ideal break down of a P + N- N + function when the structures breakdown voltage reduces (<400 V), we are no longer at electric field optimum in the structure low and now, the Rdson is related to the geometric dimensions of cells: precision of masks, lithography, industrial reproductibility of epitaxy depths and doping.

On the same graph 3, Motorola TMOS products 1982 (Δ) have been shown, product 1000 V/product 400 V/and product 100 V of chip area 30 mm².

Products 400 and 1000 V are quite far from theoretical limit $VBR^{2.5}$.

For these two products very little Rdson improvement can be made: may be a ratio of 2 within next 5 years. The low voltage device is closed to the limit Ld = 40 μm^2 with L = 2 μm and d = 20 μm.

In 1984, precision in lithography reproductibility, photoresist etch and diffusion control give the possibility to obtain d = 10 μm and L $\leqq$ 1 μm i.e. a gain of 4 on the Rdson.

Present VLSI techniques allow industrial reproduction of line thicknesses of .3 μm and mask reproductibility of 3 μm, so we can say that presently we should obtain in industrial Ld of 3 μm^2 or a reduction the Rdson by a factor of 3. This limit should last for 4 or 5 years as it consists of an optical limitation and the new X-ray machines or those with other more precise forms of alignement are being developed.

On the curve in Figure 2-68, we see that for VBR = 100 V the Rdson limit given by straight line $VBR^{2.5}$ is 1 mΩ for 1 cm².

This also means that from these geometric dimensions, only the epitaxial region resistance comes into play, which is the same for the high voltage structure.

From the curve in Figure 2-67, we get an idea of the possible improvement for the Rdson as a function of Ld.

One of the solutions that gets around the $VBR^{2.5}$ limit is perhaps to use a conductivity modulation: MOS structure with a supplementary P layer on the drain side giving hole injection, i.e. the new product known as GEMfet.

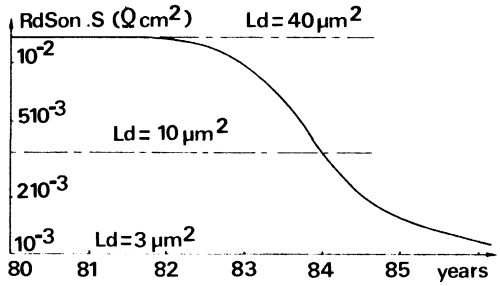


Figure 2-68 – Rdson by unit area versus years

G-2. The leakage current below the threshold voltage

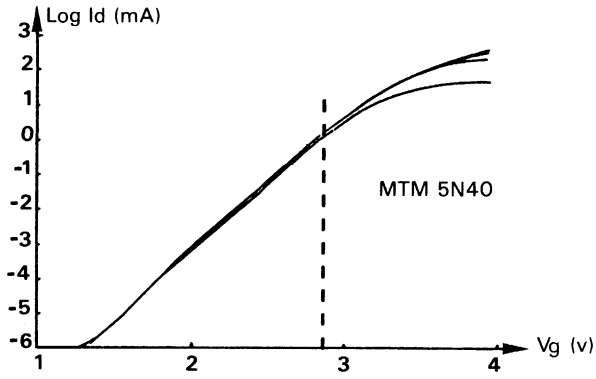


Figure 2-69 – The leakage current for VGS < 0 is very low (<10^{-9} A)

G-3. Forward characteristic $I_D = F(V_D, V_G)$

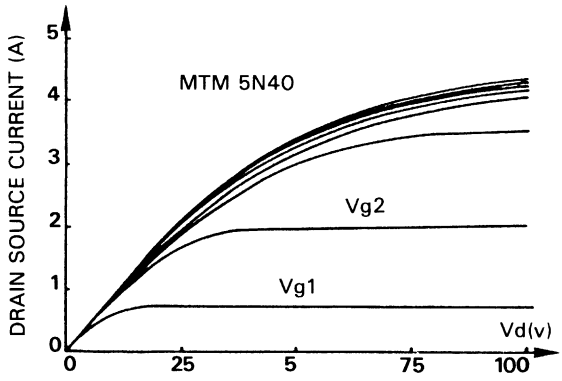


Figure 2-70 – $I_D = F(V_D) / V_G$

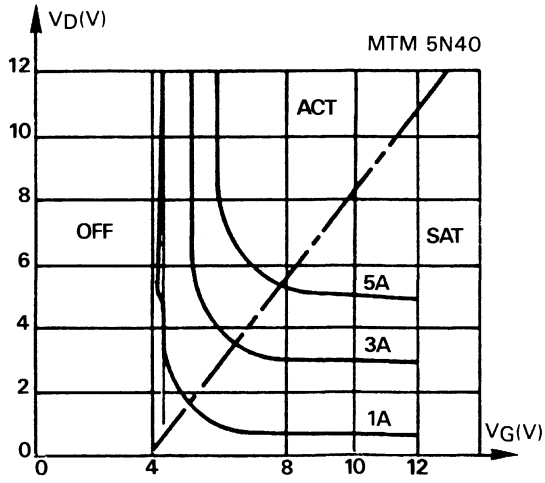


Figure 2-71 - $V_D = F(V_G) / I_D$

In fact on this curve Figure 2-71 we can spot the 3 main working regions of the power MOSfet more easily:

- the blocked region
- the active region
- the saturated region

So we can choose the MOS working point more easily in this graph.

G-4. Transconductance

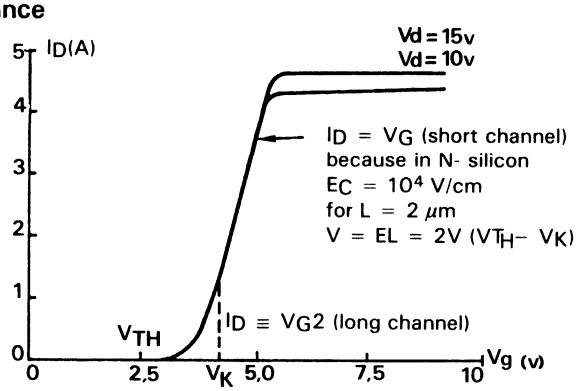


Figure 2-72 – ID = F(Va)ID

When VTH < VG < VG + 2V transconductance ID = f(VG) is in quadratic form, then ID = K .VG as in type N silicon there is a limited field EL = 10^4 V/cm so that carriers reach their saturation speed and the potential for this limited field is: V = EL = $10^4 \times 2$ μ = 2 V for L = 2 μm finally ID = cste regardless of VG the dynamic transconductance may be shown as in the following Figure.

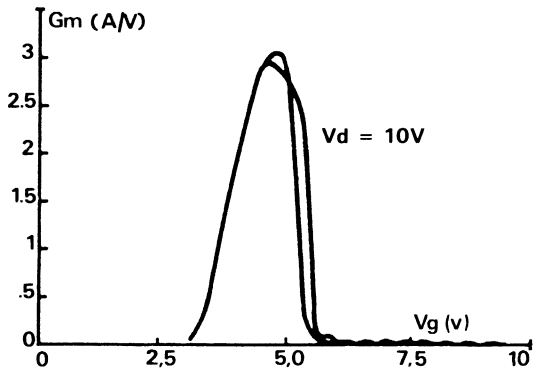


Figure 2-73 – Power MOSfet characteristics, MTM5N40

We see at this moment, that ΔID/ΔVG amplification increases, passes maximum (VG = 5V) and decreases quickly to zero after VG $\geq$ 6 V. So we see on this curve that this technology the power MOS can be used in linear power amplification only around VG = 4 V and to amplify a very small signal.

So it is clear that this type of MOSfet has been designed to be used for switching and to driven by classical logic voltage ($\cong$ 5 V).

G- 4.1. QUASI – SATURATION PHENOMENON

For low voltage power MOSfets we may observe a phenomenon called "Quasi-saturation".

Looking at bias condition No 1 (VG1 < VTH) for this condition there is little ID current and the electric field is supported entirely by the PN- junction, which extends more into the lightly doped N- region.

Then, from curves 2) and 3) for VGT2 and VGT3 in the relatively linear region of the MOSfet, the field is supported in a relatively constant manner by the N- resistance region.

The density of the free carriers is lower in ionised impurities, the N- part in the constant field acts as a series resistance with the MOS. The field in N- region increases when current increases but the rate stays the same.

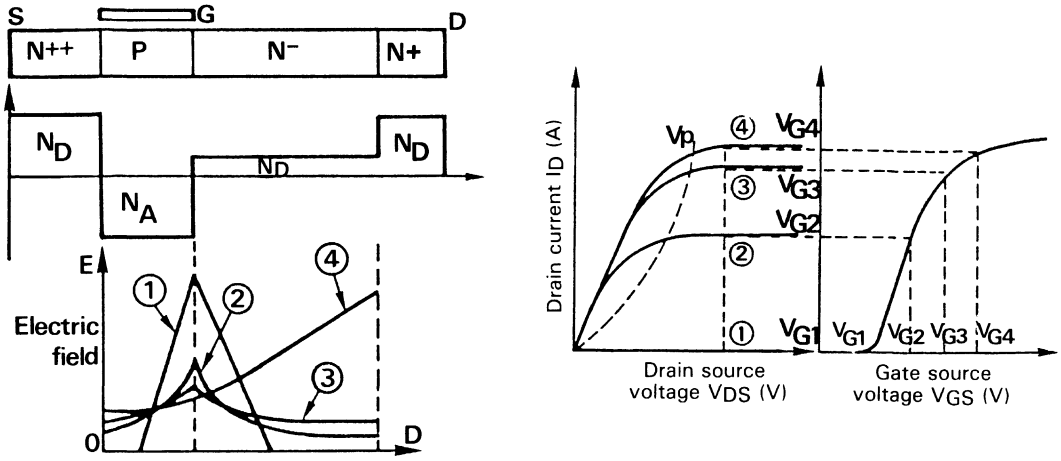


Figure 2-74

Then if gate drive increases to VG4, the field reaches critical field value (1 to 3 V/μm) above which carrier speed is constant. To ensure continuity of field between the channel and N- region the density of the N- free carrier must increase but the majority N- carriers (electrons) are moving at constant speed, an electron injection must be produced form the channel to the N- drain region. As a result, a negative space charge appears and electric field increases with the distance of the channel. The majority of voltage is supported by the drift N- region.

So series resistance of the MOS is modulated by the current and this one stays practically identical whatever the VG. (JFET)

G-4.2. Thermal phenomenon. For most power MOSfets with larger drain sections; there is an identical and continuous phenomenon, due to the increase of drain resistance with the increase in drain current: if short enough pulses are passed to avoid heating we get a much more linear characteristic (lengthing of the right hand part of the curve in Figure 2-72).

H) Safe operating areas for power MOSfets

H-1. One of the worst case overload condition that can arise in a switching product is the short circuit load at turn on when the product is still subject to full supply potential. This happens fairly often as a result of using an inverter leg (half bridge) when the reverse recovery time of the D-S diode is not negligible or when a capacitive load is switched rapidly.

Usually the wiring is minimal so that the current rise is fast: thus maximum energy exists until the safety system can protect the product. For this condition we have chosen an overload time of 20 microseconds which gives the necessary time for a classic protection system to detect the fault and turn off the system.

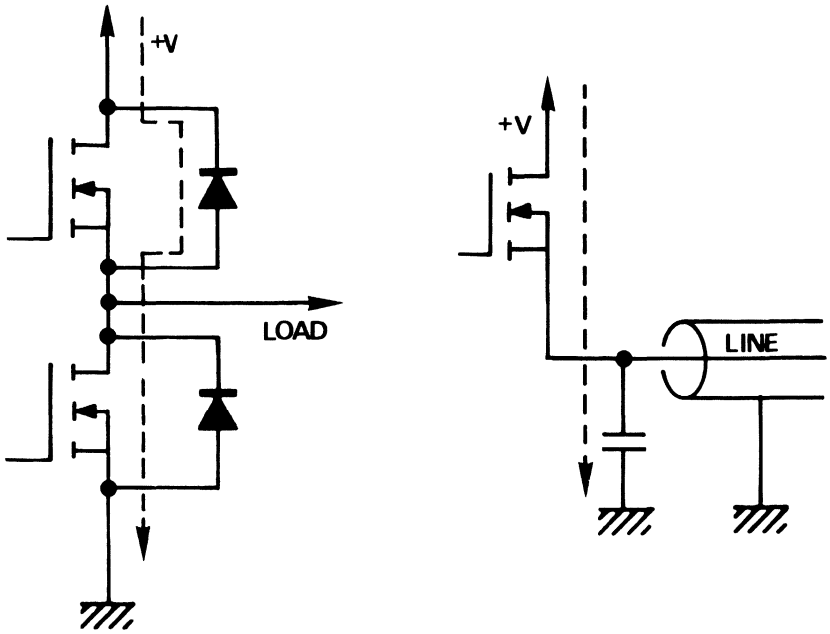


Figure 2-75 – Current overloads at turn on

If we look at VDS variations as a function VGS in Figure 2-76 we find 3 different working regions for the power MOSfet.

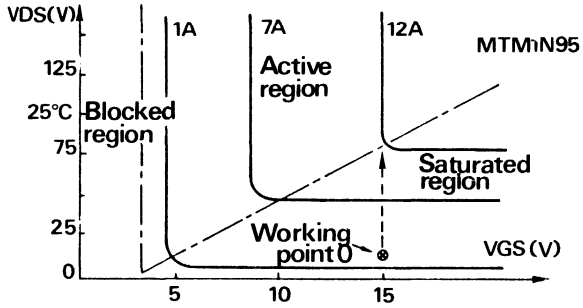


Figure 2-76 – Short circuit working point in power MOSfets

Blocking, active and saturated, for switching applications, these products are biased in order to have minimum working losses or the minimum VDS.

VDS = Iload × RDson

The bias voltage is assumed to be close to the maximum allowable (20 V) i.e. 10 V < VGS < 15 V.

When switching into a short circuit, the operating condition changes from the saturated region towards the active region and the load current is Iload = G21 × VGS for these

reasons and in an attempt to look at the worst case set VGS = 15 V and chose products with maximum transconductance (G21 or GFS).

H-1.1. TEST CIRCUIT FOR N- CHANNEL PRODUCTS

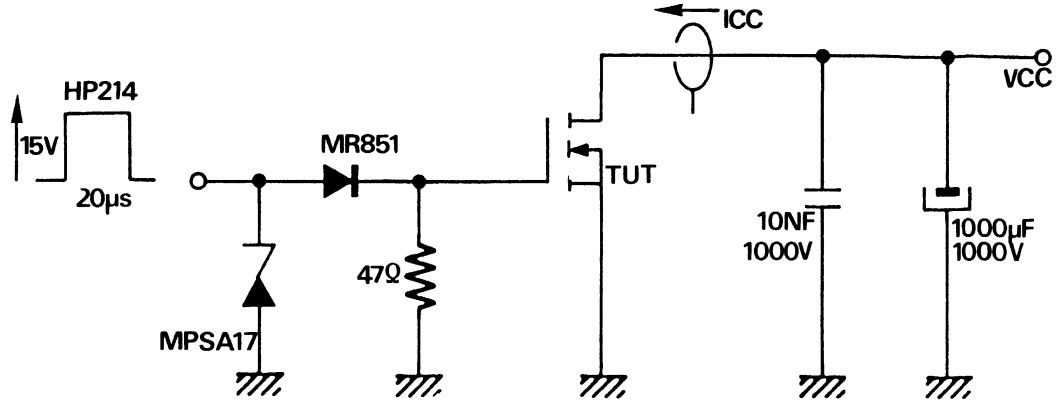


Figure 2-77 – Overload test for N- channel MOSfets

H-1.2. TEST CIRCUIT FOR P. CHANNEL PRODUCTS

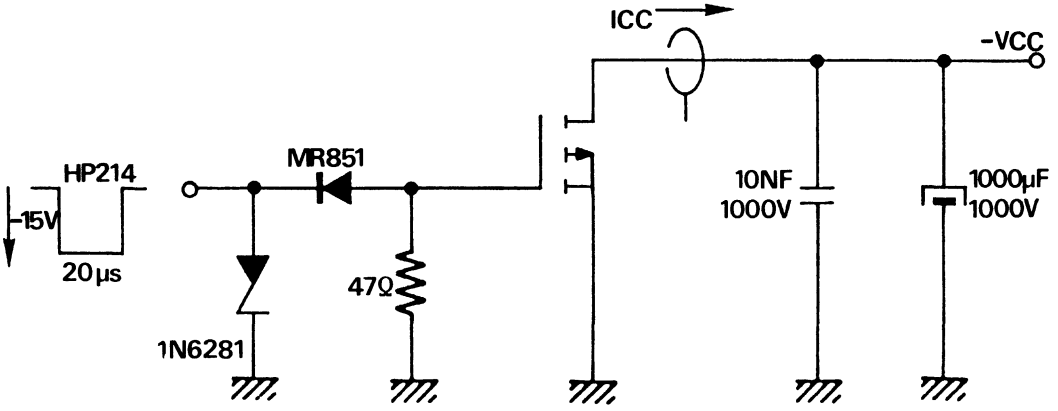


Figure 2-78 – Overload test for P channel MOSfets

We notice that these circuits have no VDS overvoltage clamping circuits in order to keep the inductance as low as possible.

Because of the current probe, there is slight overvoltage at turn off, for which was regulated in such a way that the overvoltage does not exceed the limits of the system.

H-1.3. Trial for N- channel MOSfet, low voltage MTM 12N10, 100 V, 12 A, 0.25 Ω G21 min = 3 Siemens

In this waveform we see that VDS rises to 90 V for a Vcc of 50 V and ID to 62 A for 20 microseconds, i.e. 5 times rated current and we get: $G21 = \frac{62}{15} = 4$ Siemens and

instantaneous power of 62 × 50 = 3200 W = or an energy of 62 milliJoules i.e. for a 14.5 mm² chip an energy of $\frac{62}{14.5} \cong 4$ mJ/mm² we notice a slight rise in temperature and a slight current reduction of 7% at the end of the 20 μsec pulse.

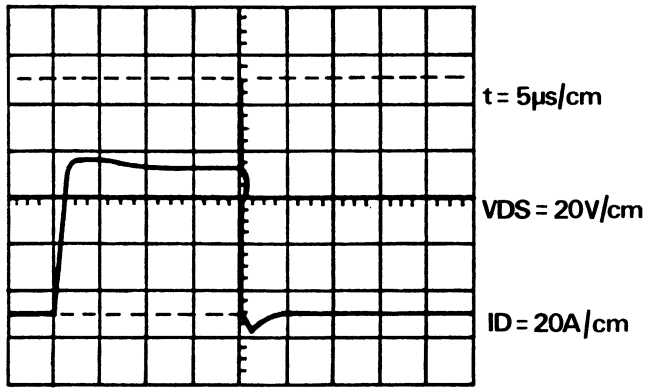


Figure 2-79 – ID/VDS oscillogram on MTM 12N10

H-1.4. **N- channel MOSfet, medium voltage MTM 15N40 : 0.4 Ω, Gfs = 6 Siemens**

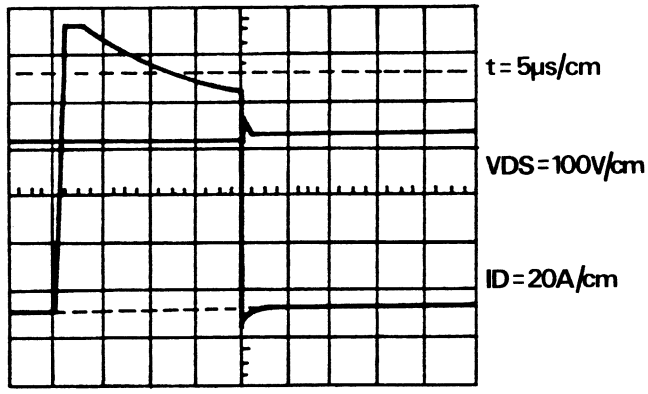


Figure 2-80 – Oscillogram ID/VDS on MTM 15N40

This 15 A device sustains 120A for 20 microseconds, i.e. an energy of 100 × 350 × 20 10^{-6} = 0.7 joules for 2 chips of 25.5 mm² each being $\frac{700}{51}$ = 14 mJ/mm².

Here, heating is much greater (14 mJ instead of 4 mJ/mm²) giving a reduction of 2/3 of G21.

On the manufacturers data sheets for this product, the transconductance graphic: Figure 2-81, at VGS = 7V Gfs varies by $\frac{27}{7}$ to $\frac{20}{7}$ from 25°C to 100°C i.e. $\Delta T = 75°C$.

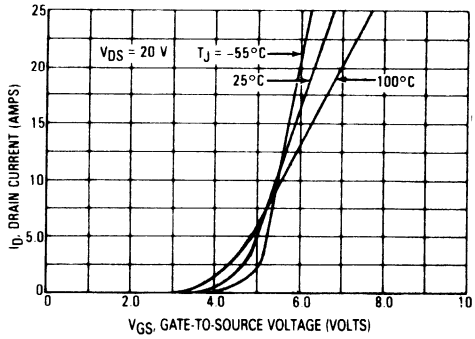


Figure 2-81 – Transfer characteristic of 15N40

If we consider, that the gfs variation follow a linear law in temperature
$Gfs\ (T°_2) = Gfs\ (T°_1)\ (1 - \gamma\ \Delta T)$
we deduce $\gamma = 0.0035$.
In this case, with a 35000 Watt pulse in 20 microseconds the current decreases from 120 to 80 A, i.e. a ΔT of 100°C.
Chip temperature decrease by 100°C during the pulse so we are below the maximum allowable junction temperature of 150°C and we do not risk degrading the device.
We can also calculate the actual thermal resistance of this product, from Figure 2-82, the transient thermal factor r(t) for 100 microseconds is shown and, if we assume that r(t) varies in $\sqrt{t}$ we can say that: r(t) at 20 microseconds is $\frac{0.02}{\sqrt{5}} \cong 0.01$.

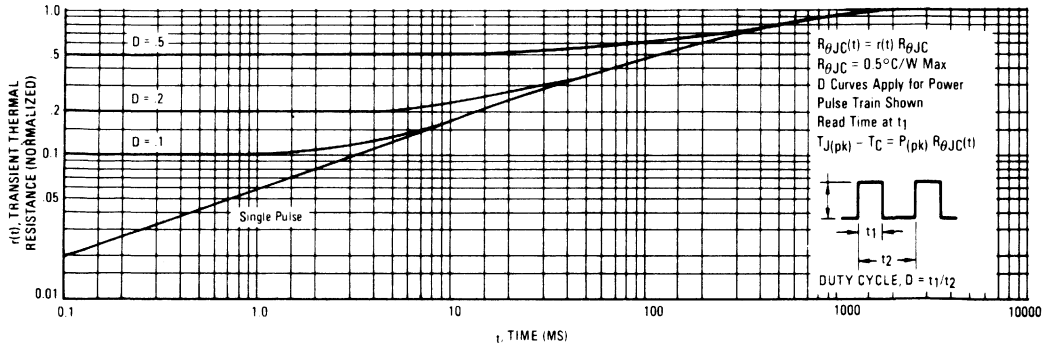


Figure 2-82 – Transient thermal resistance of MTM 15N40

Giving: $\Delta T = P.r(t)\ R\theta JC$ or $\frac{100}{35000 \times 0.01} = R\theta j = \underline{0,3\ °C/w}$

H-1.5. **N channel high voltage MOSfet MTM1N95, 10 Ω, Gfs = 0.5 S**

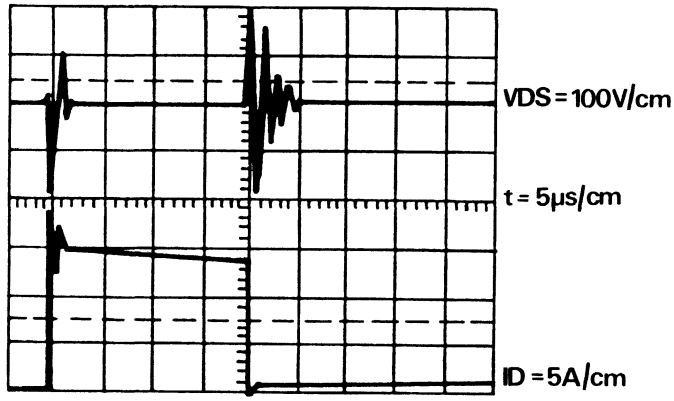


Figure 2-83 – Oscillograms ID/VDS of 1N95

This 1 A device sustains an average of 14 A for 20 microseconds and 14 × 600 = 8400 W or 168 milliJoules for a chip area of 14.5 mm² i.e. $\frac{168}{14.5}$ = 12 mJ/mm².

The heating here is such that it reduces ID from 16 to 13 A giving a ΔT of also 100°C approximately, since the temperature coefficient of transconductance is around Y = 1.7 10^{-5}.

H-1.6. **MOSfet P channel low voltage MTM 8P08, 8 A, 80 V, 0.4 Ω, Gfs = 2S**

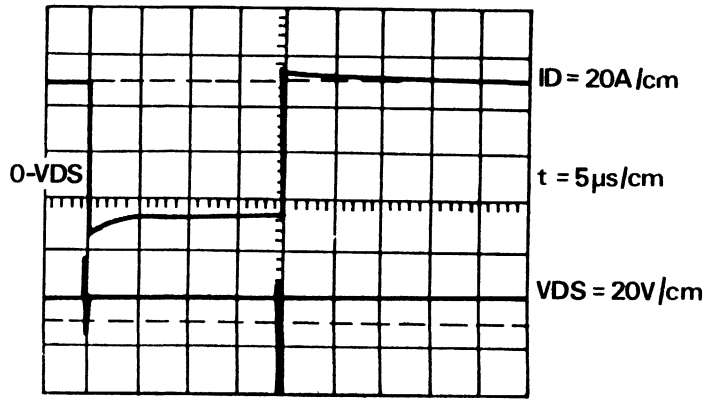


Figure 2-84 – Oscillogram ID/VDS for MTM 8P08

This device takes 60 A and 50 V i.e. 3600 W or 72 milliJoules for a 14.5 mm² chip area, i.e. $\frac{72}{14.5}$ = 5 mJ/mm², the temperature rise is low, current reduction in the order of 7% same as the N channel MTM12N10.

H-1.7. **P channel MOSfet, medium voltage MTM 2P50, 6 Ω, Gfs = 0.5 S**

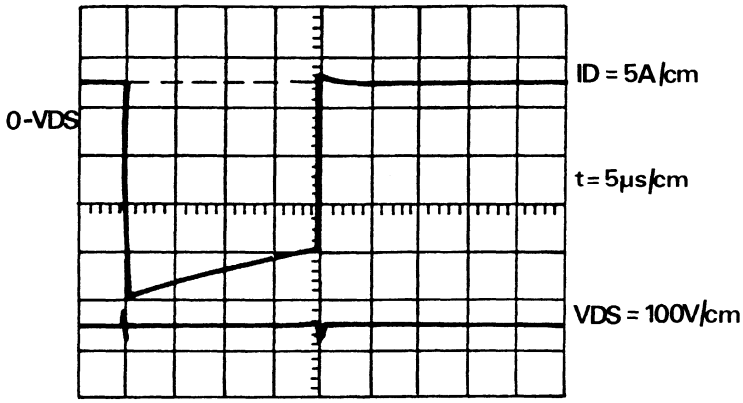


Figure 2-85 – Oscillogram I/VDS for MTM 2P50

This 2 A device takes 20 A at 20 μs i.e. 20 × 450 = 9000 W or 180 milliJoules for a 14.9 mm² chip i.e. $\frac{180}{14.9}$ = 12 mJ/mm².

The ΔT for the chip is about 80°C.

Table 2-3

		Energy (mJ)	Energy by unit area mJ/mm²	Gfs min spec 25° (S)	Mesured Gfs 25° (S)	ΔT jonction (°C)	$\frac{\text{Imax}}{\text{Inominal}}$
N channel	Low voltage MTM 12N10	62	4	3	4	30	5
	Medium voltage 15N40	700	14	6	6	100	8
	High voltage 1N95	168	12	0,5	0,93	100	14
P channel	Low voltage MTM8P10	72	5	2	4	25	7
	Medium voltage 2P50	180	12	0,5	1,3	80	10

Twenty devices of each type with high Gfs were tested several times with no catastrophic failures. These devices were then tested with continuous and dynamic parameters without showing any degradation. This would indicate then that power MOSfets can support high overload current without causing any problems with the device. However, the maximum current values given here are not guaranteed for all products of the same type for their entire lifetime. Additional tests would have to be performed to check the number of overloads allowable before the life was effected.

Under overload conditions, the junction temperature still must remain within the rated value. However, the previous analysis clearly demonstrates that power MOSfets, whether the are high, medium or low voltage, N or P channel are very rugged under current overload conditions, provided the BVdss is not exceeded.

H-2. Avalanche breakdown for power MOSfets

An initial assumption is that MOSfet product do not exhibit hot spots, or second breakdown phenomenon, which leads to the assumption that MOSfets should perform very well under high voltage avalanche condition.
The following analysis was conduct to check out these assumptions.

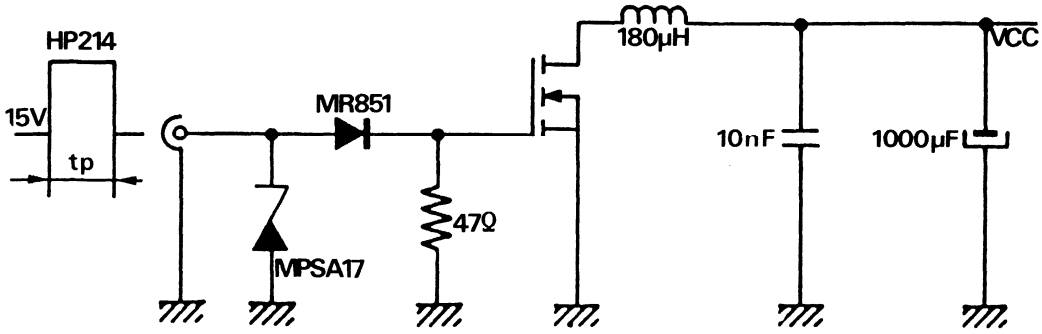


Figure 2-86 – Avalanche test for N channel MOSfets

To test P channel products, simply reverse the diagram as in Figure 2-78. A supply voltage of around VCC = 20 volts is applied and the width of control pulse tp is adjusted to vary the maximum current of ID load.

H-2.1. LOW VOLTAGE POWER MOSFET MTM 12N10 FOR EXAMPLE

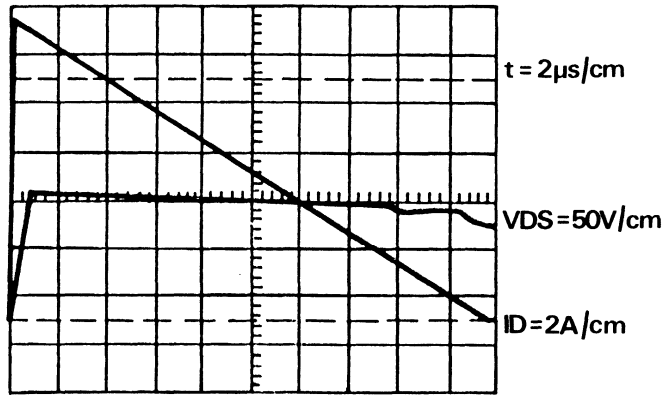


Figure 2-87 – Avalanche of MTM 12N10

From these waveforms, we see that this 100 V 12 A devices takes a 12 A 130 V for 20 microseconds giving a dissipated energy of

$$\frac{1}{2} LI^2 = \frac{1}{2} 180 \times 10^{-6} \times 12^2 = 0{,}012870 \text{ Joule}$$

H-2.2. TEST SUMMARY TABLE

Other medium and high voltage N channel products and high and medium voltage P channel devices were tested in the same way. To vary the energy sustained by the devices, either the load current or inductance was varied.

For N channel products, some did not survive even at low energy while others in the same category without high energy without destruction.

Table 2-4

Channel N types	ID nominal (A)	BVDSS specif (V)	ID min (A)	IDmax tested (A)	1/2 LI² min (mJ)	1/2 LI² max (mJ)
Low voltage MTM 12N10	12	100	2,7	22	0,6	48
Medium voltage MTM 15N40	15	400	3	15	0,8	20
High voltage MTM 1N95	1	950	/	1,6	/	1

Column ID min shows the minimum current at which some devices failed, Column ID max shows the maximum current tested which other devices survived without destruction (they may be able to sustain higher energy).

For P channel products

Table 2-5

Channel P types	ID nominal (A)	BVDSS spec (V)	ID max (A)	1/2 LI² max (mJ)
Low voltages MTM 8P08	8	80	25	56
Medium voltage MTM 2P50	2	500	8	5,7

It was not possible to find devices which failed under avalanche even when ID was increased to 4 IN and at high energy (56 mJ for the MTM8P08).

H-2.3. CONCLUSION

It would appear that P channel products do not exhibit second breakdown phenomenon. To confirm this we tested N and P channel products on a curve tracer (TEKTRONIX 576) with the minimum test time but in normal BVDSS test position.

In the oscillogram below we see that certain N channel products have a second breakdown characteristics like a bipolar while P channel products do not exhibit this phenomenon.

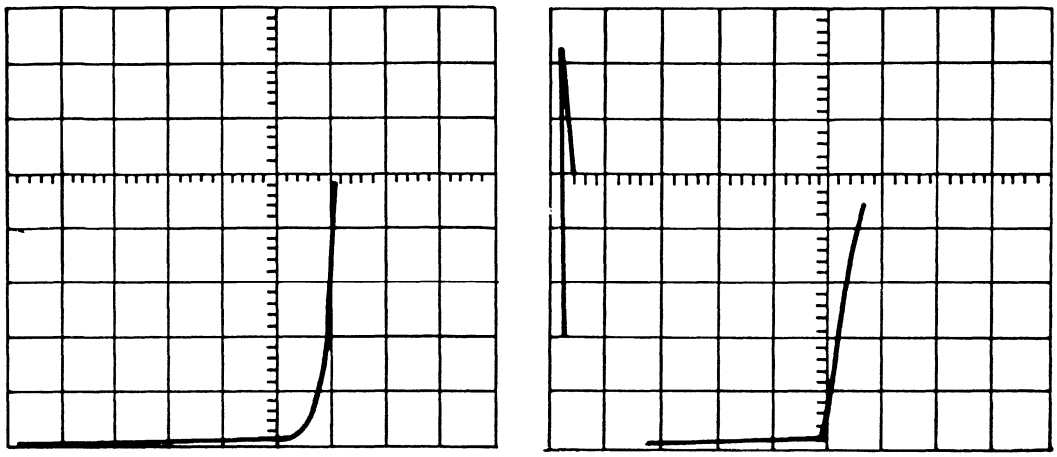


Figure 2-88 – Breakdown of P and N channel MOSfets
MTM 2P50 (P) 100V/cm – 50mA/cm/MTM 5N50 (N) time base: 1 sec

H-2.4. QUALITATIVE EXPLANATION OF THE PHENOMENON

In the text, it has already been shown that second breakdown phenomena can take place if the parasitic transistor is not sufficiently neutralized.

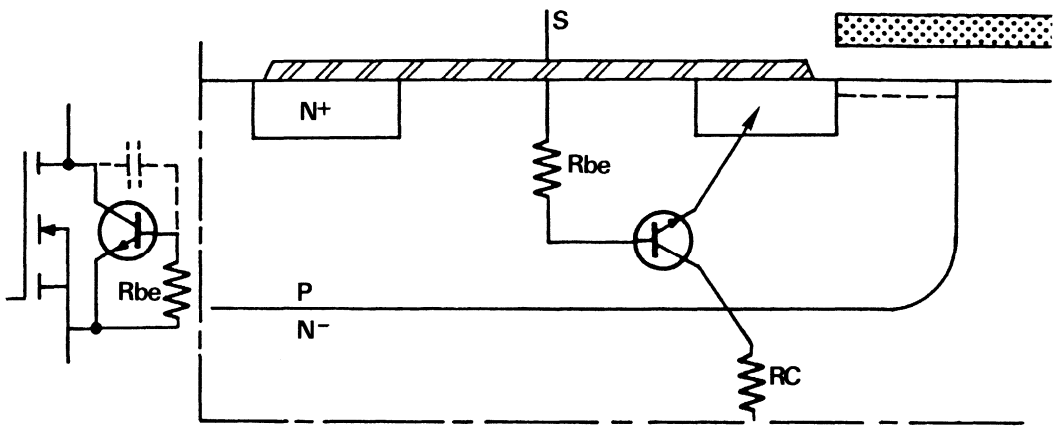


Figure 2-89 – Parasitic transistor of an N channel MOSfet

On this drawing, we see immediately that by overdoping the hole formed in N+ channel, Rbe is diminished and so the parasitic transistor is neutralized.

For example, NA = 10^{18}, l = 1 μm, s = 25 μm^2 we have ρ = 0.5 Ω .cm and Rbe = 200 Ω for a cell.

If a chip compromise 2000 cells in total, we obtain Rbe $<$ 0.1 Ω, which practically corresponds to a short circuit.

This model will not answer the question as to why certain products survive avalanche and others do not nor does it explain why P channel MOSfets survive avalanche well.

So we have to find another model.

Figure 2-90, represent the current channel in the epitaxial drift region in a N channel MOSfet, under strong electric field, (at the limit of BVDSS).

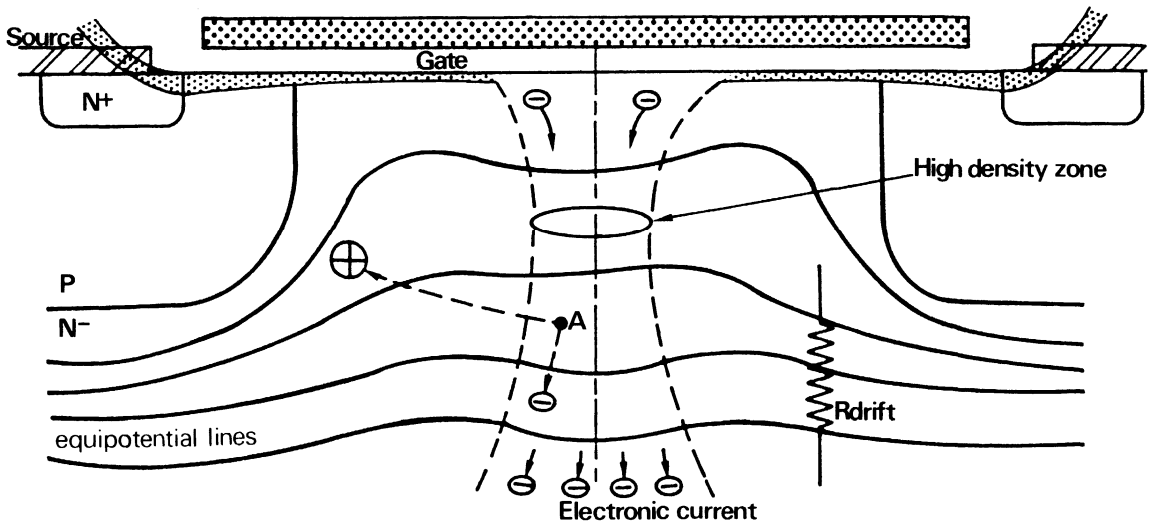


Figure 2-90 – Current channel in MOSfet and strong electric field

In this diagram we see that the electrons have high energy in the narrow region of the current channel: thus the collision of electron-hole pairs can create higher electronic density.

Because of the resistance of the epitaxial region (R drift) a low potential difference ($\cong$ 0.1 V) will enable the holes to increase electron injection from the channel. In this way we get a rapidly multiplying phenomenon and can pass into negative resistance the same as a bipolar, thus the second breakdown effect by electric field.

This effect does not occur with P channel power MOSfets, as checked in practice, as ionisation levels and multiply effects of the holes are very different from those of electrons.

H-2.5. PRACTICAL SOLUTIONS

Numerous studies of bipolar products have enabled a certain number of laws to be deduced which allow considerable improvement in second breakdown for semiconductors. Here, we can already construct the device so that the body diode breaks down before the MOSfet itself and so protects it (this diode being able to widthstand high energy in avalanche).

It is also clear that numerous research programs now being carried out on this aspect of the operation of the power MOSfet will produce a more precise model ensuring improvement of performance in N channel power MOSfet.

H-3. Conclusions

Identical tests on commercial power MOSfets with the same technology showed similar performance, so it is clear that these conclusions will apply more to the structure itself than to the devices of any particular producer. Thus we can say that power MOSfets whether:

- low, medium or high voltage
- N or P channel

Can support current overloads including short circuit loads at nominal working voltage during a reasonable amount of time (20 μs) to allow a standard protection system to reacte.

By extension, we can say that all overloads due to diode reverse recovery times or capacitive loads are very easily supported by power MOSfets provided that the maximum allowable temperature and **BVDSS breakdown voltage** are not exceeded.

On the other hand, performance with inductive loads are similar to bipolar products, very delicate, N channel MOSfets can be found that are able to support twice their rated current in avalanche for 20 microseconds and others which fail at less than 0.2 times rated current.

Recent MOSfets are already far better than the old versions in reference to this phenomenon and will continue to improve.

For P channel products, characteristics under avalanche are very good today: they can sustain 4 x In under avalanche: they are thus much better, in this area, than corresponding bipolars.

However, a very important point needs to be stressed, the **reliability** of devices which were avalanched in the tests has not been check, so the long term effect are not known. Even though the devices that survived showed no signs of degradation, it is not recommended to avalanche power MOSfets until sufficient data demonstrates this capability.

I) Switching performance of power MOSfet

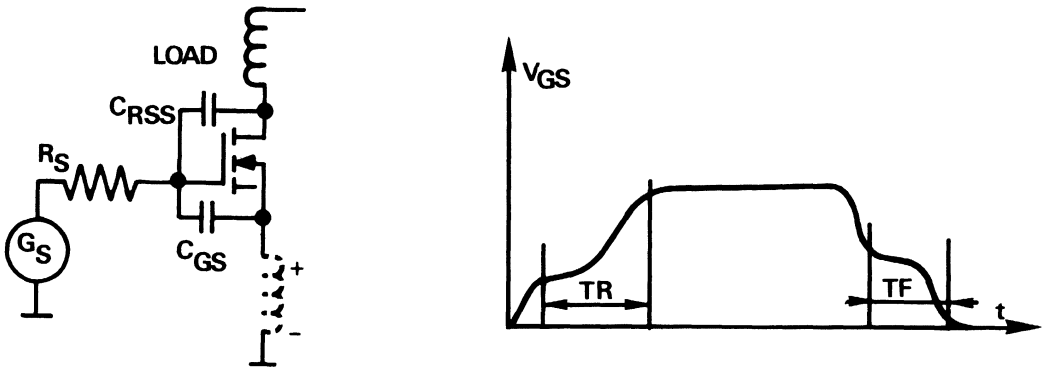


Figure 2-91

If we look at Figure 2-91, we realize that the switching performance of the power MOSfet is a function:

- of its input impedance
- of wiring
- output impedance of control generator

I-1. Input impedance of power MOSfet

We have seen before, chapter III, that the Power MOSfet has an input impedance analogous to a capacitor.

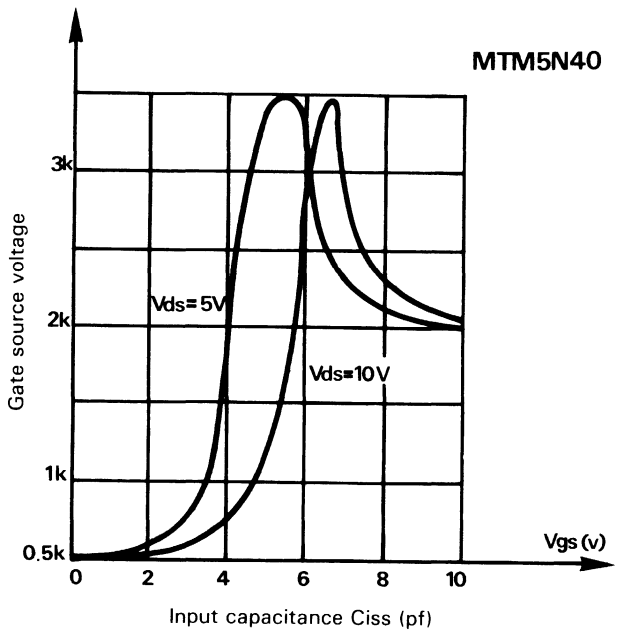


Figure 2-92 – We see here that the capacitance of the MOS viewed from input varies according to VGS

When the device is blocking, Ciss (at VGS = 0) = values given by data sheets Ciss = CGoff ≅ 500 pF for MOSs with 4 mm² area.

Next in the active region Ciss = CG sat varies very quickly for VGS > VTH and may reach ≅ 3500 pF.

i.e. CGact = 7 CGoff

then, in the saturated region Ciss = CGsat = 4 CGoff in Figure 2-93. The VGS waveform in terms of input impedance is shown.

Similar to bipolar transistors, we can define a:

I-1.1. Delay time td due to CGoff and of td = Rs CGoff Log VI/ (VI-VTH).

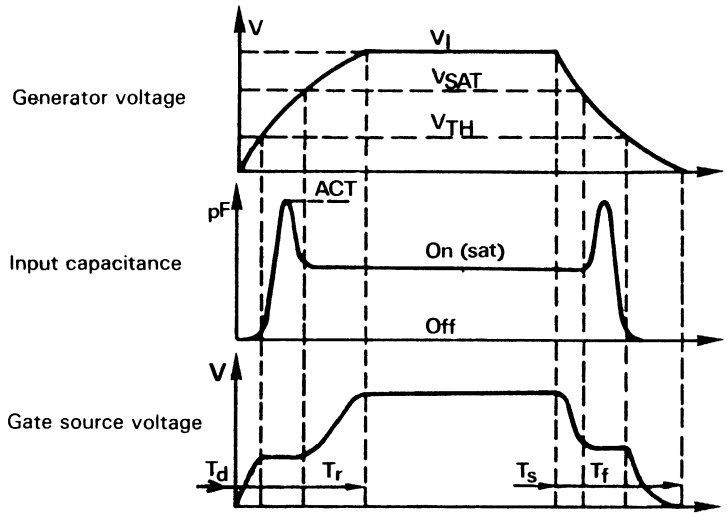


Figure 2-93

I-1.2. Rise time tr due to CGact and of tr = Rs CGact VI-VTH(VI-Vsat).

A VGS plateau is included in the rise time due to:

- dV/dt and coupling through the Miller capacitance
- wiring inductance at the power MOSfet source

In fact, this inductance will oppose all load current changes and so reduce VGS artificially at turn on and increase VGS at turn off.

I-1.3. ts storage time due to CGsat and of ts = Rs CGsat Log VI/Vsat.

I-1.4. Fall time tf due mainly to CGact and of tf = Rs CGact Log VTH/Vsat we also find the plateau here again due:

- to the Miller effect
- to the wiring inductance

I-2. Influence of the generator

The apparent output impedance of the generator obviously influences the TMOS input capacity load.

We have roughly 2 types of generator:

- A constant resistance generator (voltage generator)
- A constant source current generator which is often the case for integrated circuits

We see from this curve the influence of generator drive on switching times.

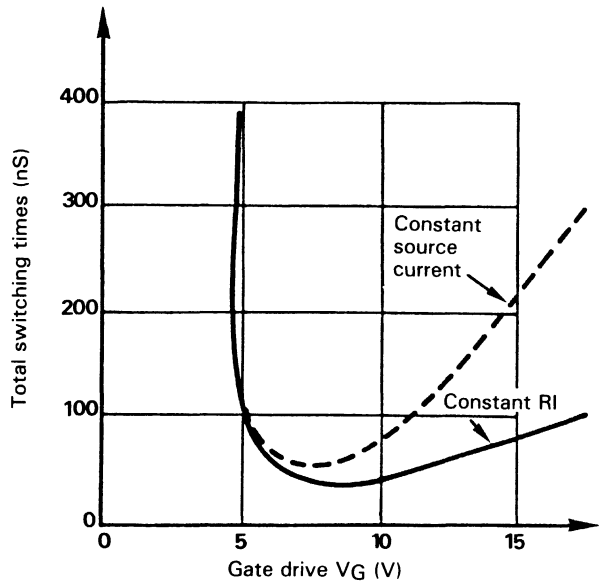


Figure 2-94

I-3. Ideal control characteristics

I-3.1. At turn on we have td = Rs Cgoff Log V1(V1-VTH) and tr = Rs CGact Log (VI-Vth)/(V1-Vsat) so we can see that to reduce these times the highest possible V1 is needed: control overshoot.

I-3.2. IN OPERATION

From the curve in Figure 2-66, we see that to have minimum operating losses, we have to work in the saturated area. (VGS = 10V)

I-3.3. AT TURN OFF

ts = Rs CGsat Log V1/Vsat and ts = Rs Cact VTH/VSAT so to minimize these times, it is necessary that V1 # Vsat # VTH i.e. a control voltage V1, be as low as possible before turn off.

I-3.4. DURING TURN OFF

We have seen (Figure 2-64), that the MOS leakage current is low, so losses are low during turn off the VTH being fairly high, the product has fairly good noise immunity.

However, Miller capacitance is high in the power MOS and dV/dt could cause problems in power applications.

So it is wise to have permanent negative VBEoff during turn off.

Example: 20 Ω generator, Crss = 500 pF, dV/dt = 500 V/μs

V gate = RI Miller = RCdV/dt = $5.10^{-10} \times 20 \times 500 \times 10^{6}$ = 5 V which is quite sufficient to turn the device back on.

I-4. Control by discrete bipolar products (MTM5N40 example)

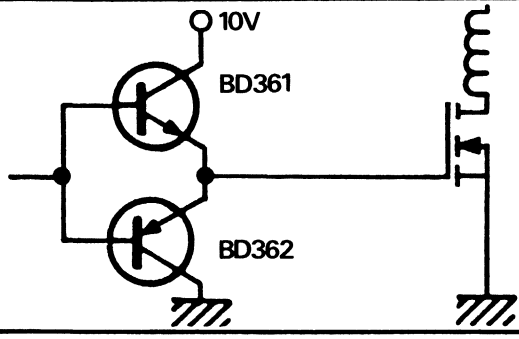
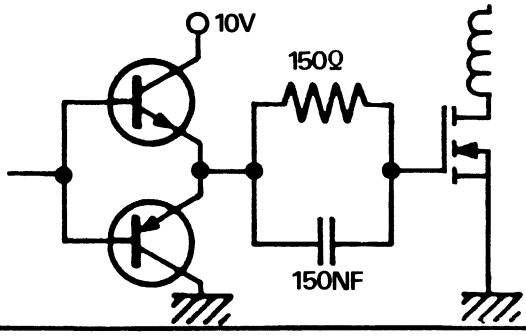
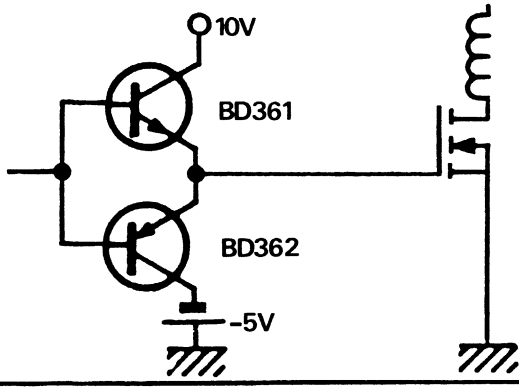
in	T_f ns	T_s ns
	30	200
	15	80
	20	80

Table 2-6 – MTM5N40

The best control is clearly with an RC circuit with no auxilliary supply, or without RC but with a 5V auxilliary supply for dV/dt immunity.

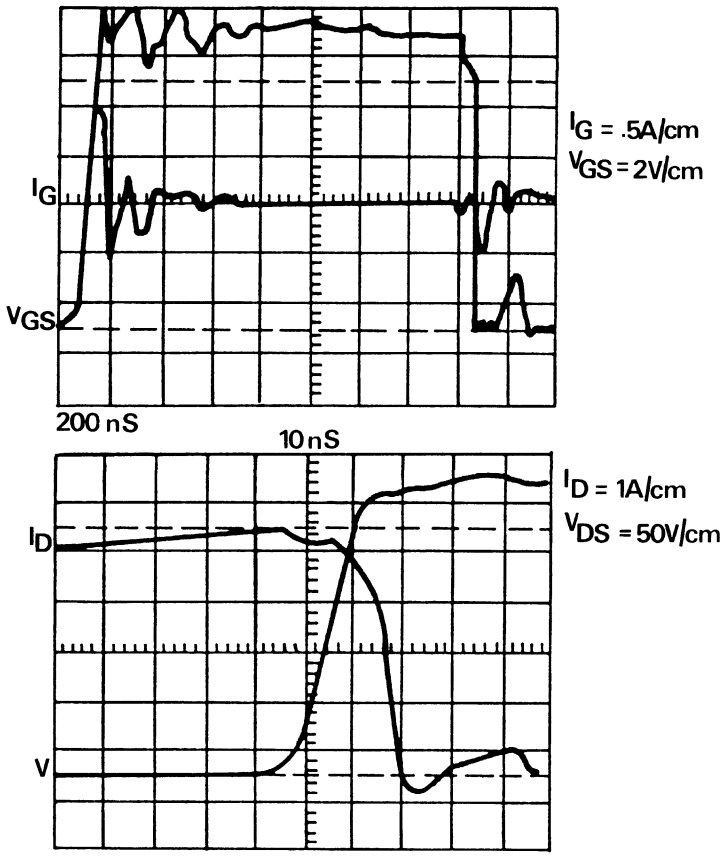


Figure 2-95 – Switching oscillograms, MOSfet MTM4N50 (100 KHz)

I-5. Control by power logic

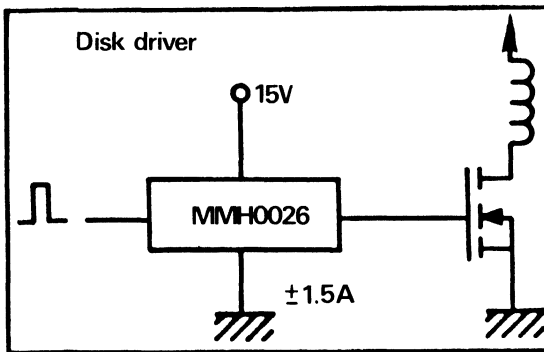
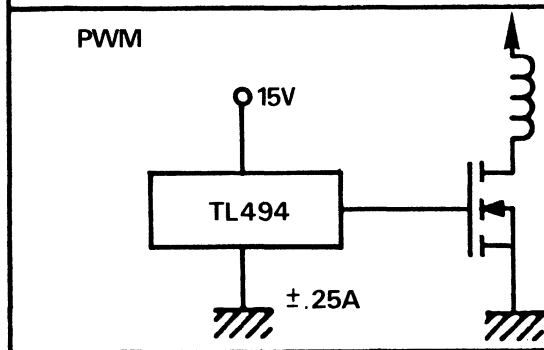
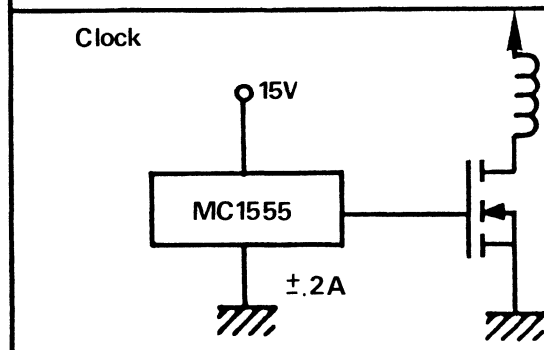
in	T_f ns	T_s ns
	20	100
	50	150
	60	200

Table 2-7 – MTM5N40

I-6. Control by classic logic

		Td	Tr	Ts	Tf
		µs	µs	ns	ns
Normal TTL 5V MC7401 330Ω		1	3	50	50
TTL-LS 15V SN74LS05 5V 1kΩ		1	1	175	75
CMOS MC14049/50 15V	1 Gate	.2	.5	1000	100
	6 Gates	.03	.04	70	40

Table 2-8 – MTM5N40 for In

I-7. Logical and discrete assembly

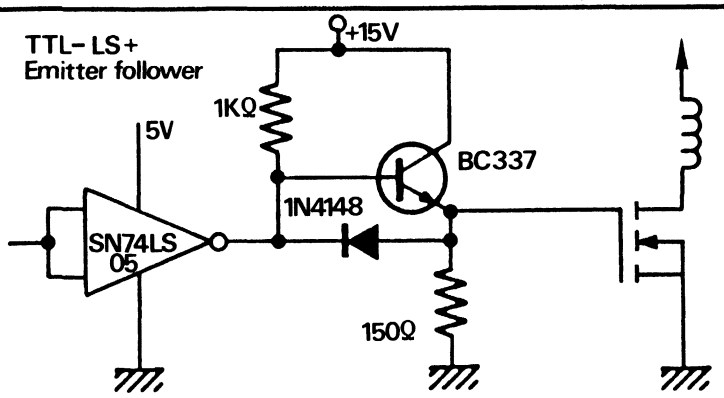
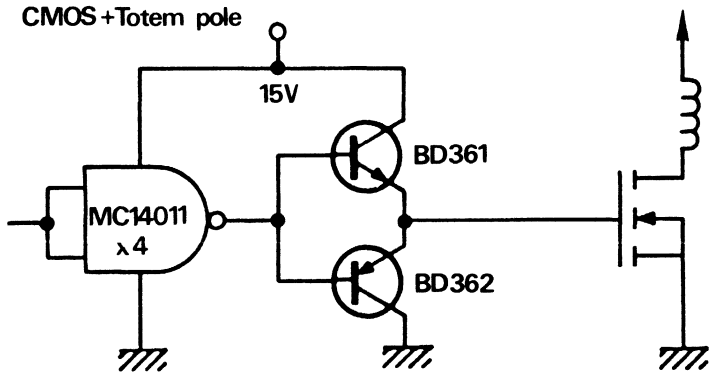
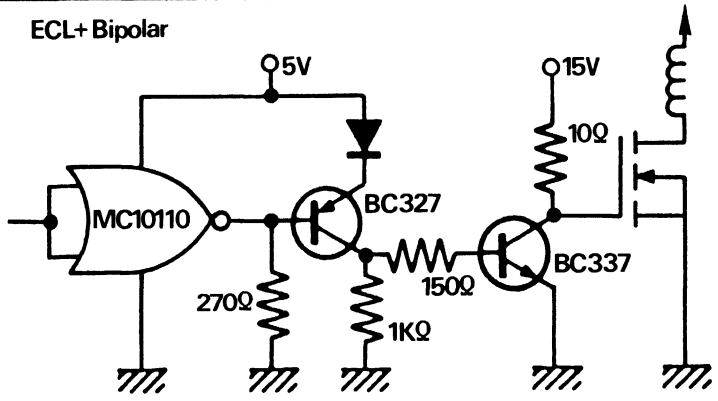
for In	T_f ns	T_s ns
	60	140
	20	150
	15	70

Table 2-9 – MTM5N40

I-8. Special controls for capacitive loads

For example a transmission line needing fast loading and unloading.

I-8.1. The first circuit is clearly a bootstrap allowing very high input impedance. Usually C ≅ 10 Ciss is chosen.

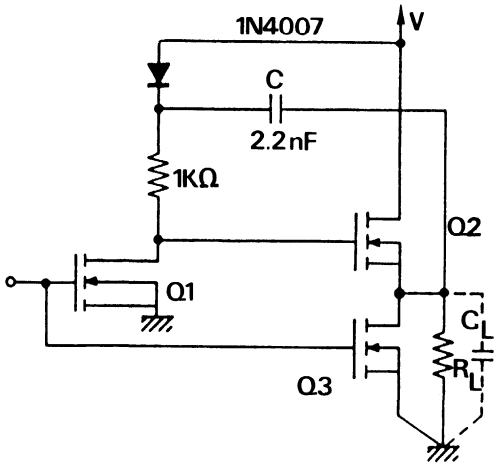


Figure 2-96

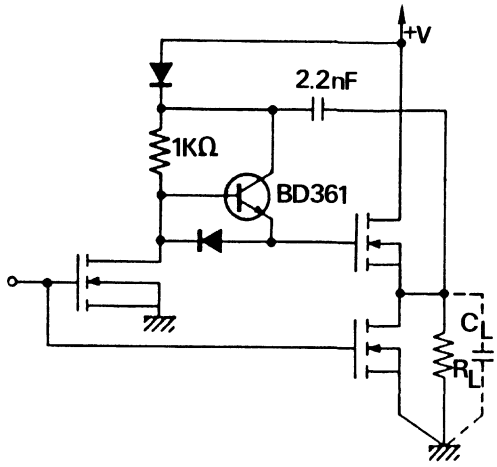


Figure 2-97

I-8.2. To further increase the pick up rate of this type of circuit, an emitter follower can be added, the small TO220 planar BD361, Figure 2-97.

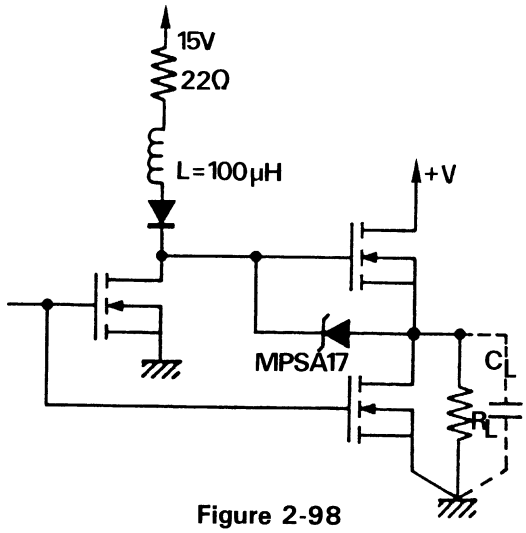


Figure 2-98

I-8.3. The energy stored in an inductance may also be used in conjunction with the zener voltage of an EB junction at 17 V (a small TO92, the MPSAI7) to keep the power MOSfet operating within acceptable load line.

J) TEMPERATURE PERFORMANCE OF POWER MOSfet

J-1. Since the input of a power MOSfet is capacitance, the switching times are only slightly sensitive to temperature.

J-2. The value of threshold voltage decreases linearly with temperature at about −6 mV/°C.

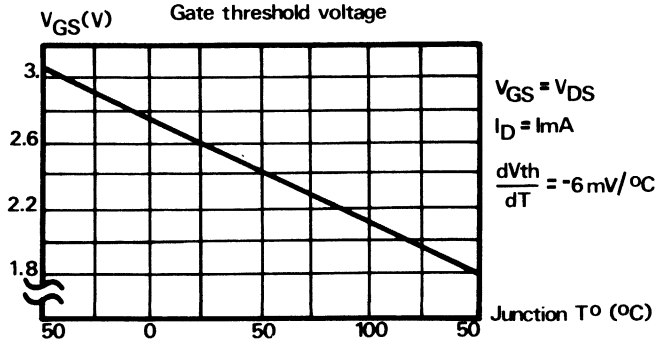


Figure 2-99 – Temperature variations, MTM10N10

J-3. Transfer characteristic ID = f(VGS) varies with temperatures.

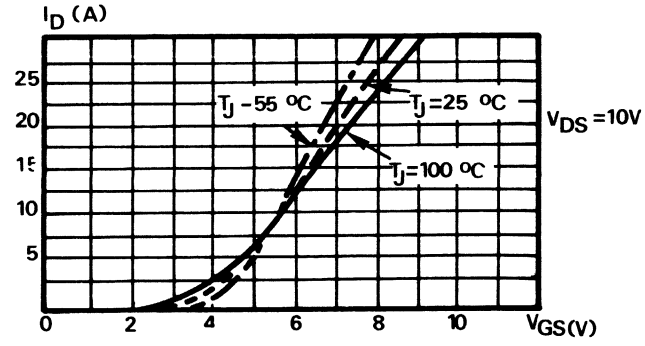


Figure 2-100 – Transfer characteristics

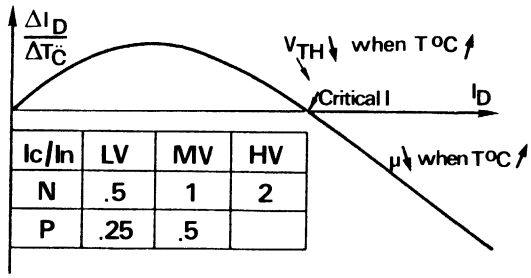
On this graph we see that below ID ≅ 8 A, ID varies positively with temperature: $\Delta ID/\Delta TC > 0$ then ID varies negatively with temperature $\Delta ID/\Delta TC < 0$.

This behaviour is true for any medium and high voltage power MOSfet. So contrary to what is usually quoted in the literature, the power MOSfet has a positive temperature coefficient for the greater part of current possibilities as in the case of bipolar transistors. How can this be explained?

From the curve in Figure 2-101, $\Delta ID/\Delta TC$ = f(ID), the positive part of the graph is due to the reduction in threshold voltage VTH when temperature increases.

Following this, the reduction in carrier mobility with the temperature becomes dominant and current reduces with temperature.

We can thus define a critical current where $\Delta I/\Delta IC = 0$ and the value of this critical current compared with the rated current of the device varies according to the breakdown voltage of the product low (LV), medium (MV) or high (HV) and according to channel polarity; P channel is less sensitive than N channel.



Ic/In	LV	MV	HV
N	.5	1	2
P	.25	.5	

Figure 2-101

J-4. The Rdson as we have seen, increases with temperature. Rdson T° = Rdson 25° $(1+\alpha)^{T(j-25)}$ see Figures 2-102 and 2-103.

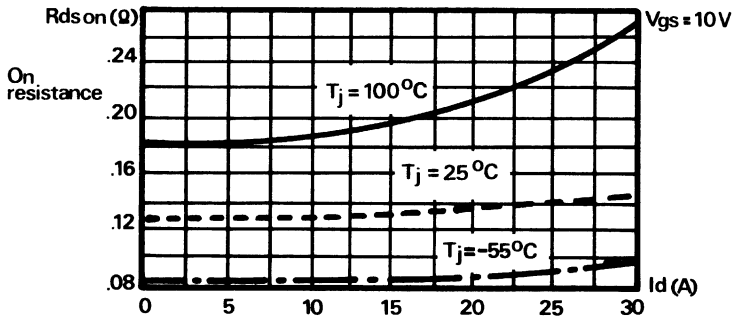


Figure 2-102

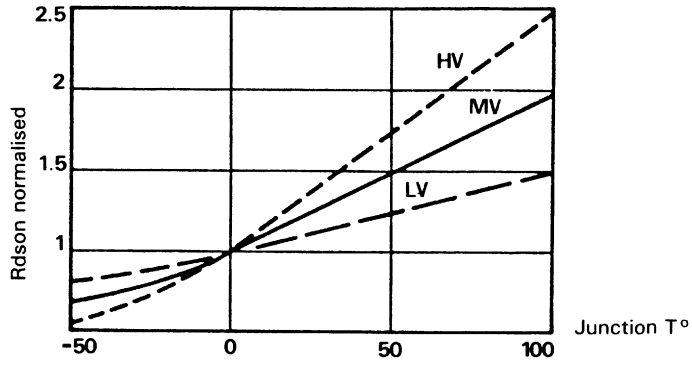


Figure 2-103

In Figure 2-103, we see that Rdson variations are not identical for high and low voltage MOSs (HV and LV). We can simplify between 25°C and 125°C ($\Delta T = 100°C$) and say

that Rdson T° = Rdson 25°C (1 + 1.5 ΔT/125) for the low voltage MOS ($\cong$ 100 V) and that Rdson T° = Rdson 25° (1 + 2.5 T/125) for high voltage MOS (> 700 V) the other medium voltage MOSfets being between the 2 coefficients.

K) Performance of the power MOSfet under irradiation

K-1. Mechanisms

Bombardment with high irradiation > $10^2 - 10^3$ rad, creates electron-nole pairs in the silicon oxides.

This same bombardment creates ionisation at the silicon oxide-silicon interface.

K-2. Radiation sensitivity

Radiation sensitivity depends on:

The thickness of Xo oxide, when this thickness is increased, radiation sensitivity increases.

The type of manufacture of the product:

- if the oxide is grown at high temperature, it is more radiation sensitive
- if it is grown in dry conditions, it is more radiation sensitive
- according to the gate metallization type (by electronic bombardment or hollowed out/melted)
- on the biasing of the product at the instant of bombardment.

K-3. Qualitative results

In Figure 2-104, we see that carrier mobility or threshold voltage decreases with the quantity of irradiation.

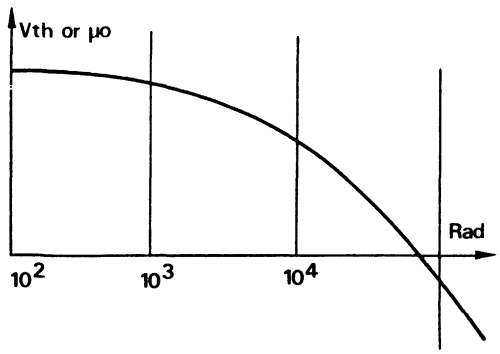


Figure 2-104

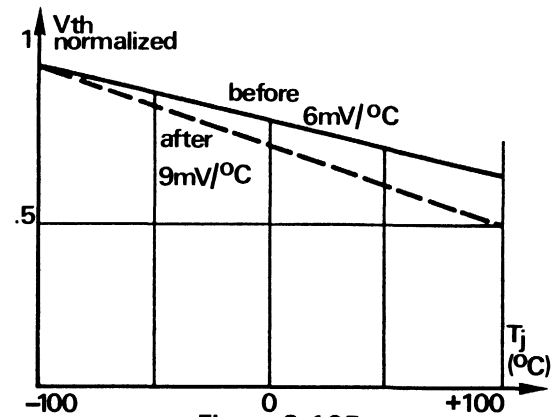


Figure 2-105

In Figure 2-105, we see that the VTH variation with temperature which was at −6mV/°C becomes −9mV/°C after irradiation.

So the MOS is more sensitive to temperature after irradiation.

L) PARALLELING POWER MOSfets

We have seen in chapter 2-D which discussed technological choices, that it was better, in economic terms, to parallel power MOSfets than to enlarge the chips. This chapter is very important, since paralleling is very often used with this type of product.
Each of the main parameters necessary for totally safe paralleling will be discussed.

L-1. Rdson variation

A manufacturing study of variations in output resistance for about 1000 devices of the same type, showed that for a 3σ (95%) confidence margin the values are at $\pm 20\%$ of the mean value. This means that current variations will also be $+20\%$.
However this condition will be self correcting because the lowest Rdson device will carry the maximum current, and will increase in temperature, thereby increasing Rdson thus ID will decrease and balancing out the ID sharing.
Therefore Rdson variations are not therefore a problem when paralleling.

L-2. Variations of $I_D = f(VG)$ transconductance

We can equally look at the problem of transconductance variations, VG being identical for all products, ID variations equal that of GM.
Here also we have undertaken a manufacturing study for a certain number of pieces and we conclude that ID varies at $\pm 20\%$ which is not real problem if there is good thermic coupling and even in worst case conditions these products can support an overcurrent of $\pm 20\%$ without damage.

L-3. Variation of threshold voltages (VTH)

When paralleling power MOS for switching applications, it is important that all devices

switch a the same time, otherwise a low VTH device may carry a large portion of the load-current while the other devices are off.

The only solution to this problem, is to apply a stiff drive voltage which was already recommended for good turn on of a single device (paragraph I-3).

L-4. Thermal problems

L-4.1. In the case were the control device itself limits the load current (linear amplifier is an example), the device with the heaviest load heats up more then the other device (for the case of paralleling two devices) and thus it's Rdson increases. The increase of Rdson tends to reduce the loads and balance the sharing of load current good thermal coupling is very desirable because it tends to automatically balance the system.

L-4.2. In the typical case, where the load determines the current which the power MOS must supply (the case for all switching applications). If Rdson increases with temperature, the current remains stable, but the losses increase with increasing temperature and there is thermal drift. The solution is to have an adapted heat sink.

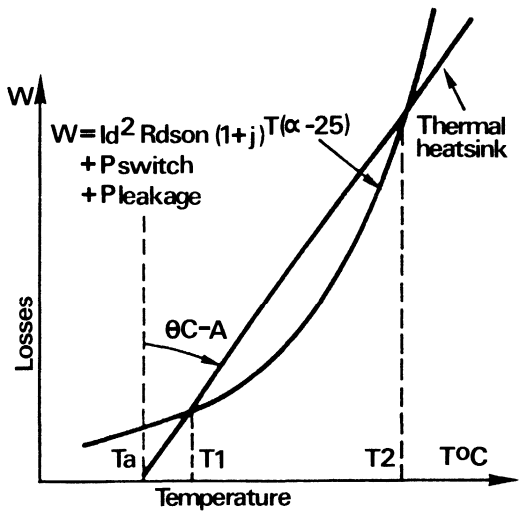


Figure 2-106

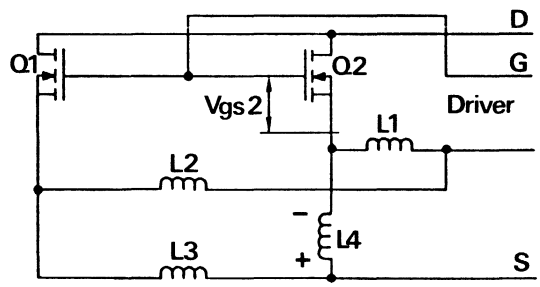


Figure 2-107 – Lay-out problems

The total losses in the power MOS shown Figure 2-106 are: W = I_D^2 Rdson $(1+\alpha)^{(Tj-25)}$ + P switching + P leakage and there is a stable point in T1, but if for some reason.

The ambient temperature increases (Ta increases) there may no longer be a stable point thus resulting in a thermal drift.

The junction to ambient thermal resistance increases: i.e. air flow is stopped or obstructed, which increases the slope of θ c-a resulting in a possible thermal drift.

L-5. Layout problems: Figure 2-107

If the wiring in paralleling system is composed of different lengths L1 = L2 = L3 = L4, there may be sufficient induced voltages to trigger the device in the parallel combination when they are suppose to be off. In fact, taking a difference in wire length of 10 mm, its inductance is $\cong 10^{-8}$ Henry and if the current is 5A with 10 nanoseconds (10^{-8}s) switching time, we get roughly: $dV = L\ dI/dt = 10^{-8}.\ 5.\ 10^{8} = 5$ V

In addition good wiring has a compensatory effect on variations off threshold voltages (VTH).

Let us suppose in effect that L1 = L2 and L3 = L4 and that VTH2 > VTH1.

Q2 will want to turn-off before Q1, but L4 will artificially increase VGS2 and keep it in conduction.

L-6. Parasitic oscillations

Power MOSfets have a fairly high cut-off frequency, considerable Miller capacitance, high power gain and negative output impedance at certain frequencies. All this means that these devices have a normal tendancy to oscillate. If mounted in parallel, the slightest imbalance of loop impedances causes the system to oscillate. Therefore, great care must be taken when paralleling these devices.

If the system should oscillate, there are several empirical solutions which may be used separately or together:

- a resistance of 10 Ω to 100 Ω in series with the gate
- ferrite beads on power MOSfet terminals
- drain source capacitance

Remember to keep connections as short as possible.

See following diagram.

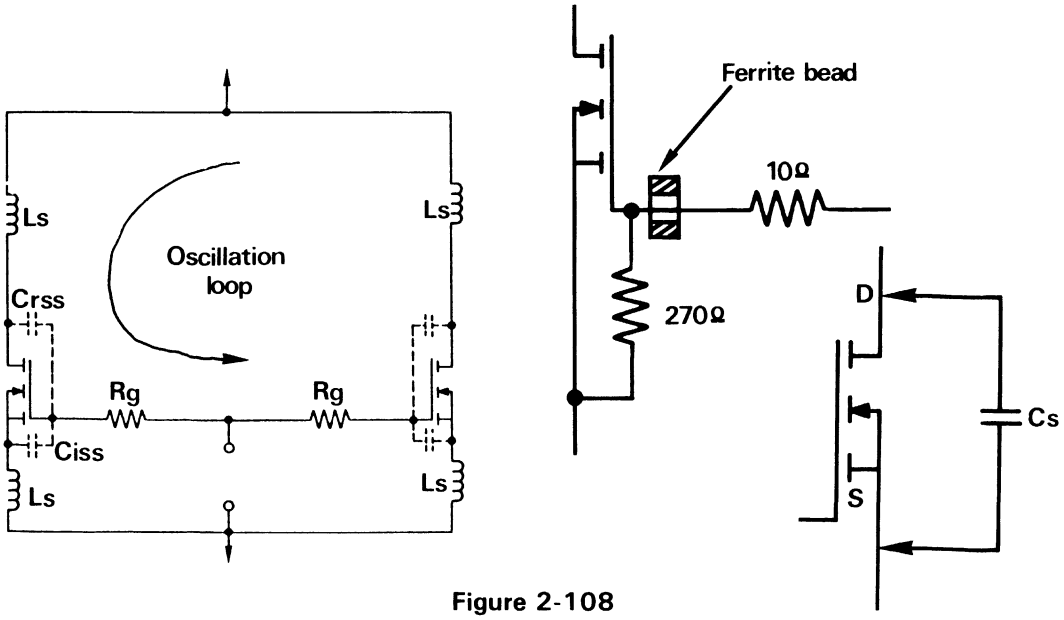


Figure 2-108

M) Protection of power MOSfets

M-1. Gate protection: Figure 2-109

The best protection is a zener at power MOSfet input which limits VGS < VGSmax (≅20V).

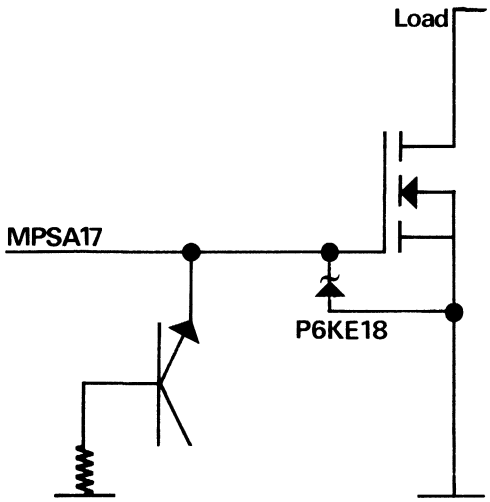


Figure 2-109

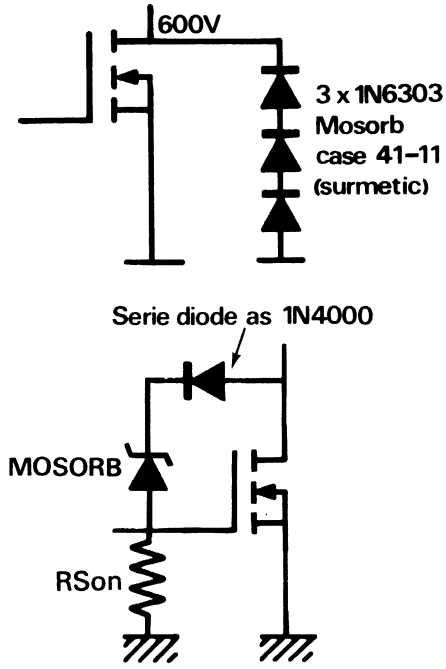


Figure 2-110

There are some power MOS devices on the market with a zener integrated into the gate, but it does not generally perform well because this integrated zener diode creates a parasitic transistor. One solution would be to use a standard zener with VZ = 15 V but standard zeners usually have a non negligeable capacitance which adds to the MOS input capacitance.

One solution is to use a zener diode formed by the emitter-base junction of a small plastic TO 92 transistor with planar technology. Which has a zener voltage of approximately 15 V, and very low capacitance (1-3 pF).

We could use also a transient suppressor as MOSORB P6KE 18 (surmetic package).

M-2. Drain-source protection: Figure 2-110

The best drain-source protection at the present time is the power zener diode called the Transient Suppressor type MOSORB (1N 6281A, etc.)

We could use also this zener diode between Drain to Gate in serie with a normal rectifier diode as 1N4000.

N) Future of the TMOS

The future of the power MOS may be defined mainly in relationship to:
- its cost compared to other products with the same performance
- its losses, especially in the on state, thus its Rdson

N-1. Costs

The problem is fairly simple, if we compare a power MOSfet with a power bipolar we realize that all the important phenomena of these devices take place:
- at the surface (channel) for power MOSfets
- at the bulk (base) for bipolars

Since the density of crystal defects (dislocations, impurities) is considerable at the surface (Figure 2-111), it is assumed that the production yields of power MOSfets will always be lower than those of bipolars.

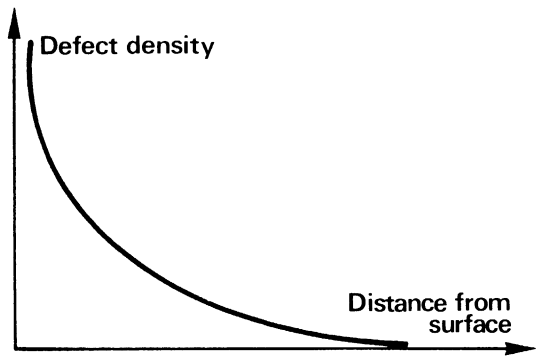


Figure 2-111

So the technological price of power MOSfets at the present time is greater than that of bipolars for identical silicon area.

N-2. For Rdson

Figure 2-112 show the equivalent resistance per unit area for power MOSfets and bipolars (gain of 10), verses the breakdown voltage of the devices.

We see from these curves that the equivalent bipolar Rdson is better than the theoretical curve for high voltage power MOS. So there is little chance, that present day high voltage MOSfets will compete with the fastest bipolars for switching application at frequencies < 100 KHz.

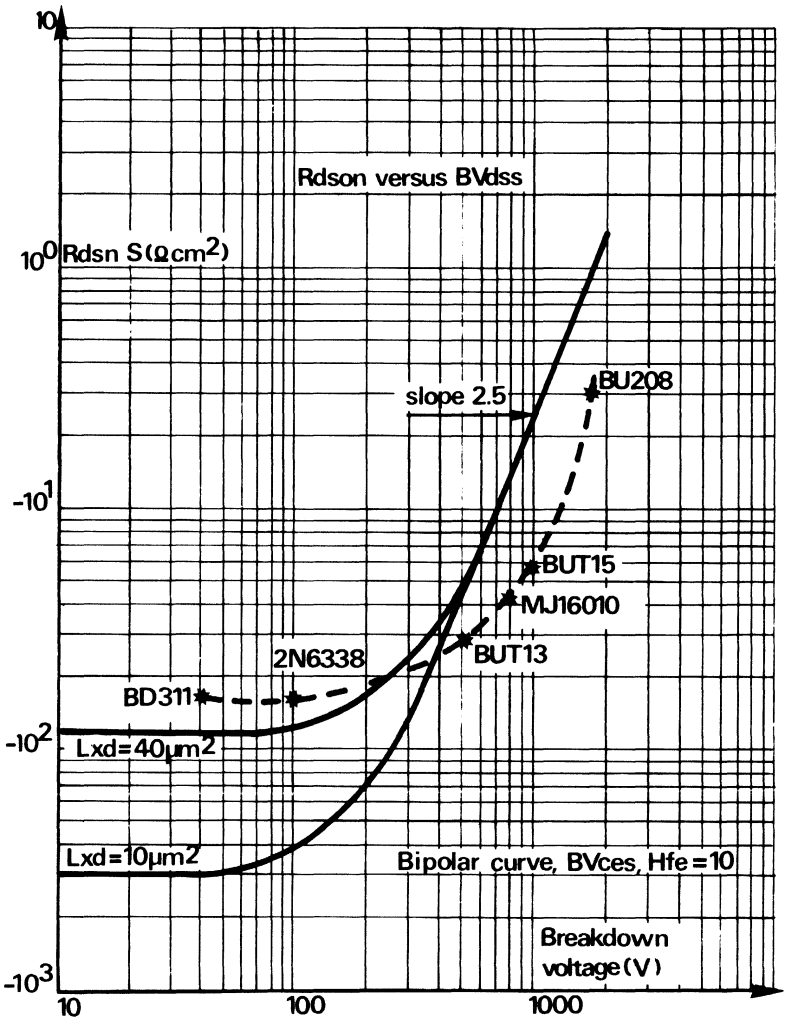


Figure 2-112

O) Conclusions

O-1. As we have seen, that low voltage MOSfets (< 200 V) with high current ratings have a good future in:

- telecommunications
- and traction and leverage systems (combustion engine car, electric car)

And in switching operations:

- switching times are independent of temperature
- control energy is low

For use as a relay:

- control is very simple
- energy controlled is practically zero (direct control by logic)
- good reliability

O-2. Medium voltage power MOSfets (200-500 V) may be used when the transfer of large amounts of energy is the overriding factor, regardless of economic considerations.

O-3. High voltage power MOSfets (> 500 V) with present technology, are useable for applications, where:

- large power transfer, and
- volume reduction (high frequency) are of primary importance compared to cost

However, improvements in technology and techniques for power MOSfets, such as the MOS Thyristor or the Gemfet with conductivity modulation, could changes things in the near future, see the following chapters: 3 and 4.

P) Bibliography

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- Le compromis entre la résistance à l'état passant et la tenue en tension dans les transistors MOS de puissance, Thèse de 3e cycle – Tien Phan Pham – Toulouse 1982
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3. The MOS Thyristor

A) Introduction

The biggest disadvantage of medium and high voltage power MOS is its on resistance Rdson. In fact Rdson is proportional, to breakdown voltage for a DMOS structure.

$$\text{Rdson} = \frac{k}{s} \text{VBR}^{2.5}$$

For high current applications, the area(s) becomes large which tends to produce lower than desirable production yields. For example if I = 15 A and Rdson = 0,1 Ω at 25° C and V_{br} = 600 V. Then (S) theoritically would have to be ≧75 mm².

The only other alternative is paralleling which is both expensive and touchy. A way around this disadvantage was found with the development of the MOS thyristor which allows this theoretical Rdson limit to be significantly reduced for a given silicon area.

A brief look at how this device is manufacturer, it's basic function electrical characteristics, and applications.

B) Technology

In this figure, the classical cellular structure of a DMOS device can be seen with its horizontal channel and vertical current. However, a supplementary layer P+ has been added below the DMOS (drain) to create the thyristor anode.

Looking at the small vertical hatched band area, the classic vertical structure of an SCR with 4 bands and 3 junctions can be seen N+ – P – N- – P+.

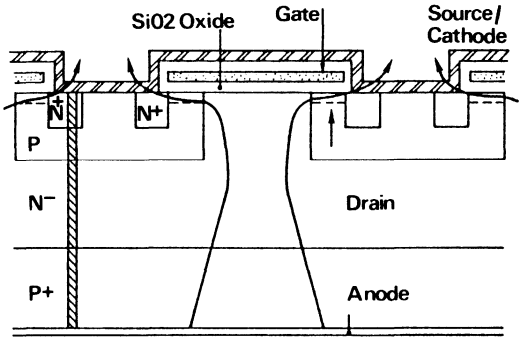


Figure 2-113 – Crossection of a MOS SCR

So, if sufficient current is generated in the classical MOS structure to cause the injection of holes from P+ region, we then have a regenerative effect which gives a low voltage drop in the on state.

This structure can be represented symbolically as shown in Figure 2-114.

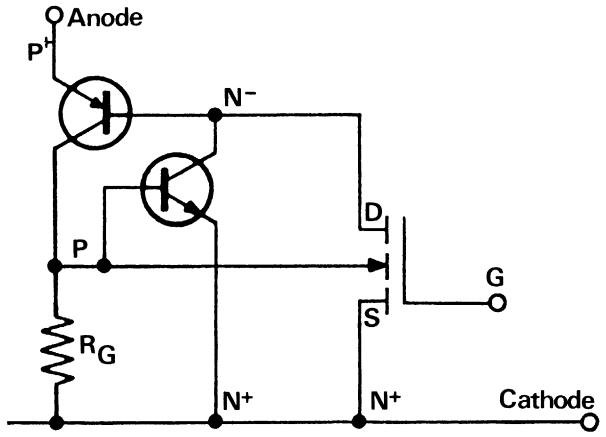


Figure 2-114 – Equivalent circuit of MOS Thyristor

In this figure it is easely to recognize the self-blocking combination of the two PNP and NPN transistors.

The MOSfet is turned on by a gate to source voltage of approximately > 3 V, the resulting drain current provides the base current of the PNP transistor which turns on and supplies the base NPN transistor. This creates a loop gain conditions > 1 and the regeneration phenomenon of an standard thyristor starts:

$$\alpha 1 + \alpha 2 > 1$$

The MOSfet can now be turned off = VGS = 0, but the SCR stays on as long as the load current stays above the minimum holding current.

In reality, the turn on phenomenon of the system is slightly more complex, particularly the R_G resistance which must be optimised (P well resistance), because it can cause two different turn on possibilities:

- either, as stated above by the NPN/PNP combination
- or by biasing of substrate with the single PNP transistor

This turn on mode can be produced in discrete elements with small MOSfets and an accessible substrate.

To optimize this resistance, the channels which connect the source to the P wells can be widened.

The proposed symbol for this MOS thyristor is shown in Figure 2-116.

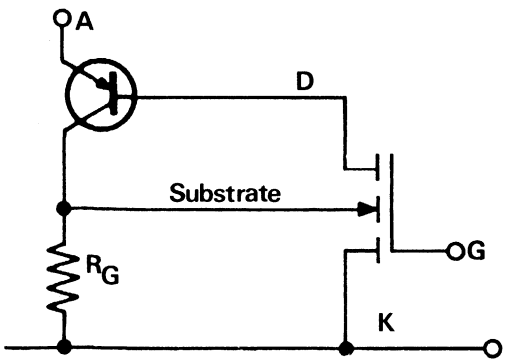


Figure 2-115 – Turn on by substrate

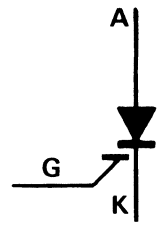


Figure 2-116 – Symbol

C) Static characteristics

On a curve tracer the MOS thyristor has as VI characteristics as shown in Figure 2-117.

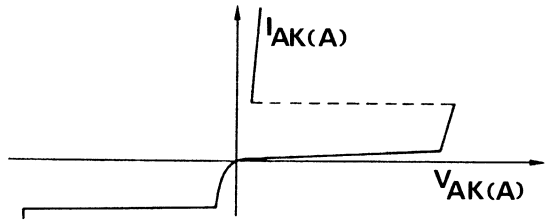


Figure 2-117 – Characteristics of MOS SCR

The classical curve of a standard SCR can be seen in quadrant 1. In quadrant 3, this device exhibits a fairly high leakage current (> 10 mA) and is an asymmetrical device.
For the MCR1000 with silicon area of area of 14 mm², and commercially available from Motorola.Other static characteristics are:

Typical V_{TM} = 1,3 V to 20 A Rdson equivalent of 1.3/20 = 0,065 ohm.

The latching current is IC = 350 mA and holding current I_H = 25 mA. Minimum VGK control voltage is 2.5 volts which guarantees good noise immunity.

D) Dynamic characteristics

D-1. One dynamic characteristic of an SCR is its blocking time, during which it cannot be forward biased again or it will start conducting again. This time is known as tq; this for subject device is around: tq ≅ 4 microsecondes.

However, recent experience indicate that tq's of between one and two microseconds are attainable.

D-2. Another significant characteristic of SCRs is the dI/dt at turn on: due to the multicellular structure of this MOS thyristor maximum surface area is turn on in a minimum time, and numerous tests have shown a capability of dI/dt equal to 100 A per microsecond without any detrimental effects to the device.

D-3. SCRs are generally used in circuits with high dV/dt potential gradients.
The blocking capability is obviously a function of the gate biasing and the dV/dt curve verses resistance Rgk is shown in Figure 2-118.

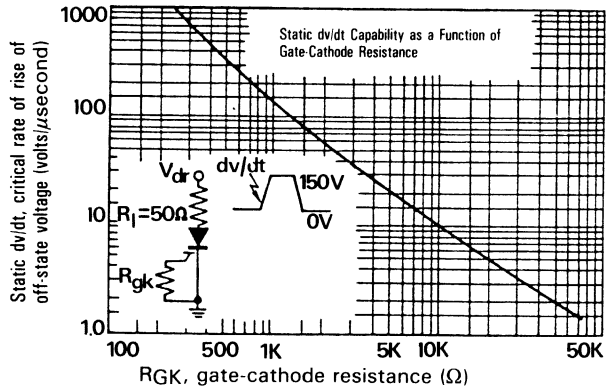


Figure 2-118 – dV/dt verses gate to source resistance

Due to the voltage threshold V_{GTH} of the MOS thyristor of ≈ 2 V, there is improved dV/dt capability over the classic SCR structure which has a turn on voltage of about 0.6 volts.

E) Control of MOS SCR

The main advantage of the MOS SCR compared with a normal SCR, is that it can be driven at low power level (high input impedance), thus they can be controlled by classical logic devices.

E-1. CMOS gate MC14011

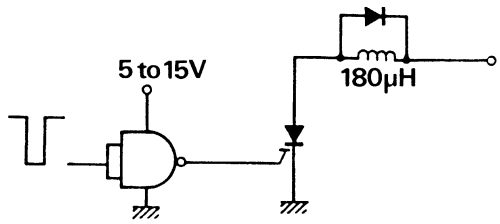


Figure 2-119 – Control by CMOS gate

Since this circuit delivery only several milliamperes (< 10 mA) of drive current, turn on time is fairly long.

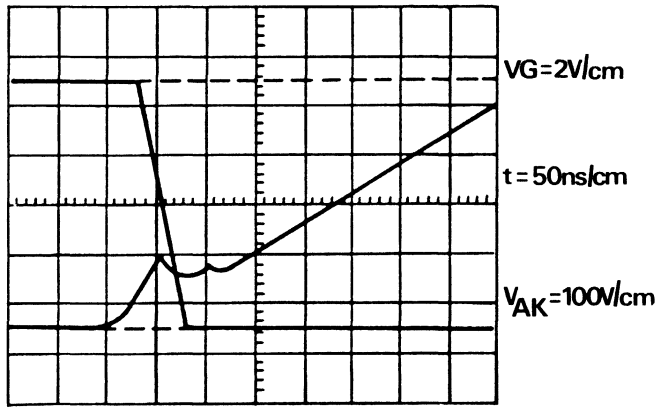


Figure 2-120 – Turn on with a CMOS gate

In paralleling the 4 gates available in a single package. The drive capability is increased by a factor of 4 (~ 30 mA) and turn on time is improved.

30 nanoseconds instead of 50 nanoseconds

If a 6 gates "Buffer" MC 14049 device is used, 80 mA is available and thus better dV/dt immunity, with turn-on time still being very good.

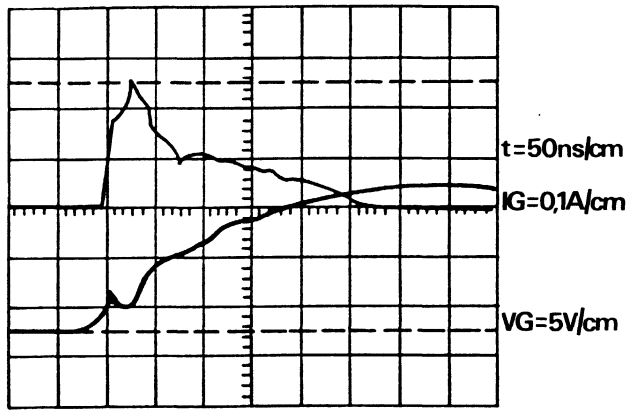


Figure 2-121 – Gate characteristics with a MC 14049

E-2. TTL-LS gate 74LS00

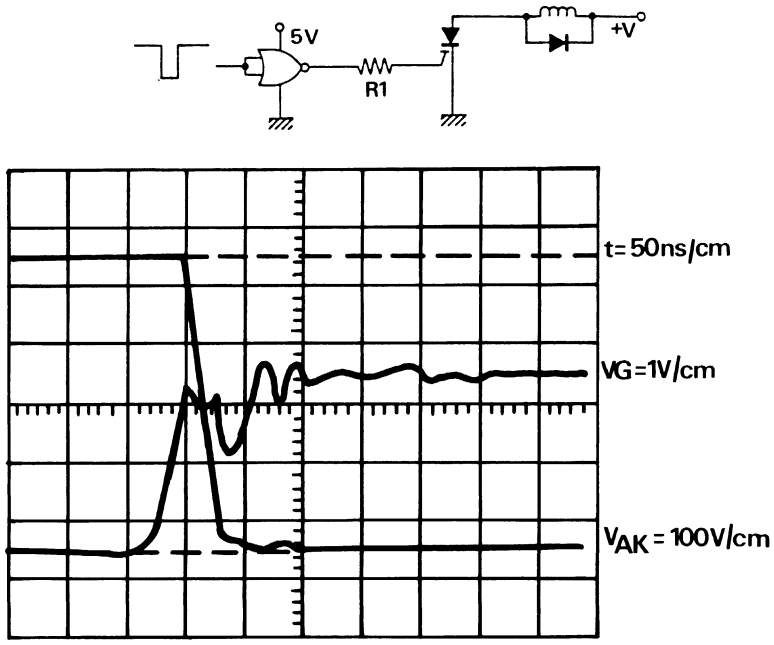


Figure 2-122 – Control and turn on characteristic for 4 × 74LS00 gates in parallel

E-3. Table 2-8, shows turn on times with various logic devices and biasing conditions.

Table 2-13

Gates Ic's and supplies	Delay time t_d (ns)	Rise time t_r (ns)
MC14011 at 5V supply	200	80
MC14011 at 15V	40	25
4 × MC14011 at 5V	60	35
4 × MC14011 at 15V	15	15
MC14049 at 15V	30	25
MC14049 at 5V	125	70
6 × MC14049 at 15V	15	15
MC74LS00	35	60
4 × MC74LS00	20	20

E-4. Figure 2-123, shows how switching times vary as a function of R1 gate resistance.

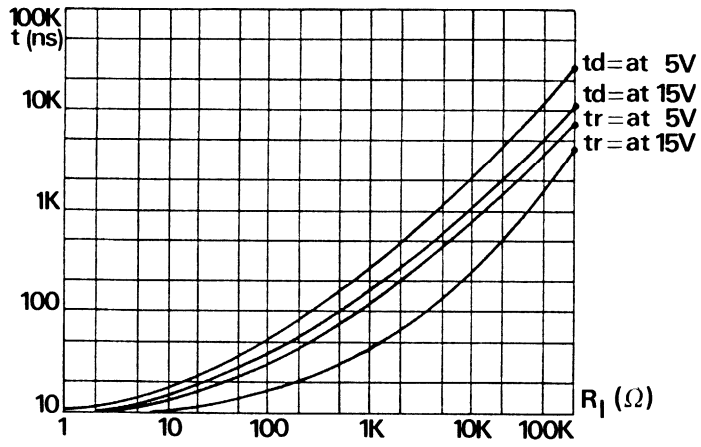


Figure 2-123 – Switching times as a function of R1 series resistances

F) Applications

F-1. Rectification at 50 Hz

When turning the device on during a half sinusoïd at 50 HZ (10 ms), an important parameter is the angle of non-conduction.

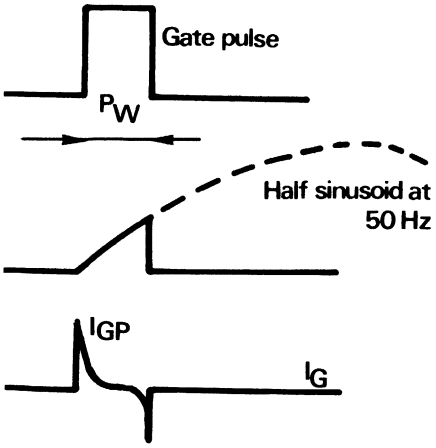


Figure 2-124 – Minimum control angle Pw

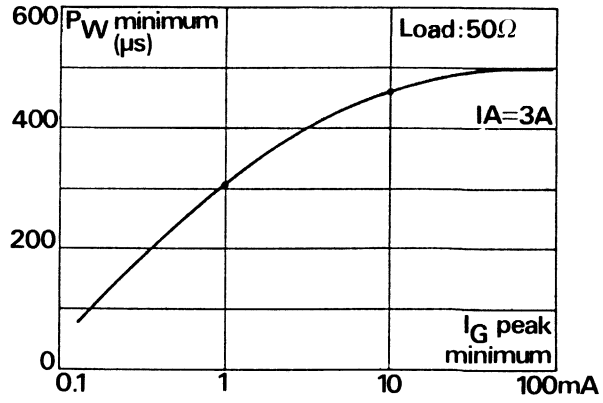


Figure 2-125 – Minimum control for a sinusoïd arc passing through zero

If the MOS SCR is controlled by a Ic's gate, it becomes clear that the law which gives the minimum of peak current in the gate or the minimum pulse width to turn on the device is rather surprising.

In fact, the minimum gate current must be increased in order to turn on the device when the control pulse width increases; normally the reverse would be expected in terms of quantity of charge needed for charging the MOS SCR capacitance.

However, be looking closely at the equivalent circuit (Figure 2-126) it can be seen that with low gate impedance the MOS is turned on quickly at a low Rdson impedance short circuits the NPN transistor, decreases $\alpha 2$ and thus slows down the systems blocking conditions:

$$\alpha 1 + \alpha 2 \leqq 1$$

So for the minimum loss angle, a fairly high gate resistance is necessary (100 kΩ).

To maintain good dV/dt immunity, it is important to have the minimum gate impedance – see the following optimum diagram for turning on a MOS SCR with a sinusoïd.

The capacitance is included to reduce delay time at turn on.

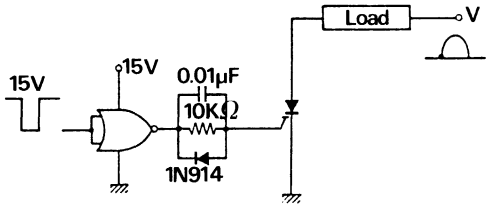


Figure 2-126 – Optimum control diagram

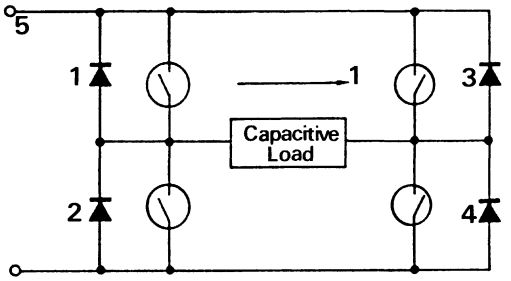


Figure 2-127 – DC/AC convertor

With this network there is a delay time at turn on of td = 40 nanoseconds a rise time tr = 90 ns, and a loss angle of about 200 microseconds, i.e.

$$\theta P = 0.2/10 \times 180^{\circ} \cong 4 \text{ degrees}$$

with a loadcurrent of 3 amperes.

F-2. Switching in the converters

F-2.1. If the load is capacitive, there is no problem, it's the ideal device because it has the minimum of losses and switching occurs naturally: Figure 2-127.

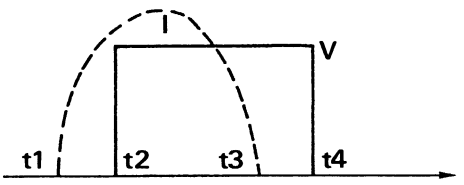


Figure 2-128 – Voltage current oscillogram in capacitive load

When the MOS SCR is fired at time t2 Figure 2-128, there is enough current to insure having I_L.
When it passes to t3, the current reduces to zero and the MOS SCR blocks.
Voltage reversal in t4 occurs when the MOS SCR is fired.
F-2.2. If the load is inductive, the following simple and economical converter may be used.

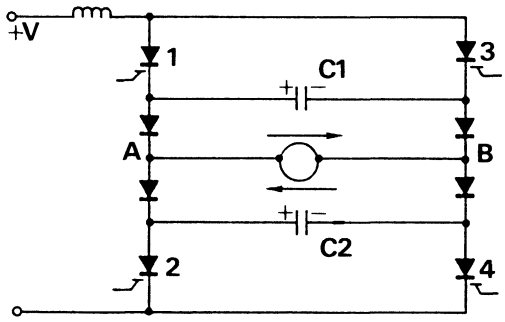


Figure 2-129 – Monophase converter

If T1 and T4 are conducting and it is required to turn them of to reverse the current, simply fire T2 and T3, C1 and C2 being automatically charged by the system, the current circulates in T3, C1 D1, D4, load, C2, T2 and the current cancels itself in T1 and T4, and they automatically turn off (low losses).

Once the load current has reversed the voltage at C1 and C2 terminals, D1 and D4 block, VB potential rises, current circulates from B to A through T3, D3, D2 and T2, → Load current is reversed.

This system makes it possible to have a high current commutator (SCR) which is very efficient (few losses at turn on, turn off or in operation), the diodes protect the MOS SCR against possible reverse conduction.

With the MCR 1000-6 (600V-15A) loads of 5 to 6 kVA can thus be controlled.

G) Conclusions

This new technology, which combines the qualities of power MOSfets and SCRs looks promising for the future. This device makes it possible to control the main power switch using a small amount of energy (MOS) without creating prohibitive voltage drop in on state (Rdson).

The only disadvantage is blocking, but with the help of technical progress, it will be possible in the near future, to reduce the tq to less than a microsecond, and so, provide the market with fast device that is rugged easy to operate, and cost effective.

H) Bibliography

AL PSHAENICH 1982 "The MOS SCR, a new Thyristor Technology" – Motorola EB 103

RJ GODING 1982 "MOSfet offers low on resistance" Electronics, Dec. 15

4. GEMfet

A) Technology

If we look at the MOS SCR technology, that is to say the cross section of a TMOS device with an added P+ layer on the anode side. This additional layer allows injection of holes into the N- epi region along with the electrons brought by gate bias. The result created is a structure with conductivity modulation.

The equivalent resistance, in conduction, of this structure becomes much lower than that of a classical TMOS power transistor where a single type of carrier participates in conduction.

Evaluating the equivalent circuit containg the MOS and the bipolar transistors which make up the structure, shows a latched system if the gain is high enough (TMOS-SCR). An unlatched system or GEMfet (Gain Enhanced MOSfet) results with lower gain.

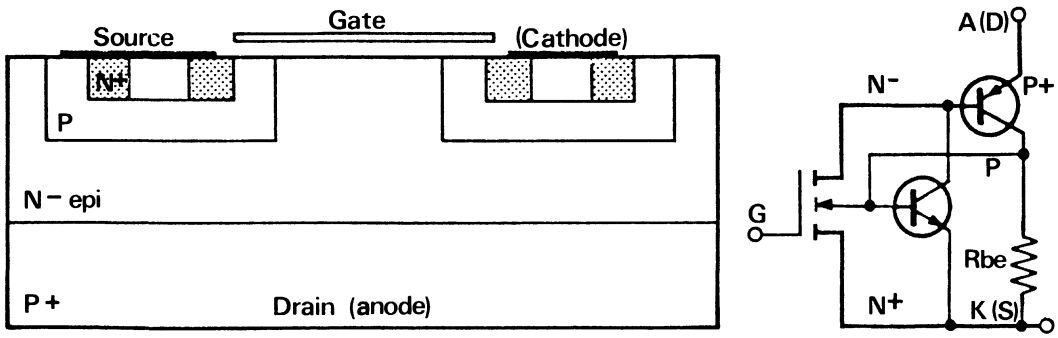


Figure 2-130

According to the preceding figure, the GEMfet can be considered as a Darlington composite PNP/TMOS, the NPN bipolar part being considered as a parasite.

For this it is necessary for the NPN transistor to have a very weak α and the RBE resistance is as low as possible i.e.:

- N+ source slightly doped → N
- P+ of wells (substrate) very heavely doped P+ +.

If we compare the 3 structures, we obtain Figure 2-131.

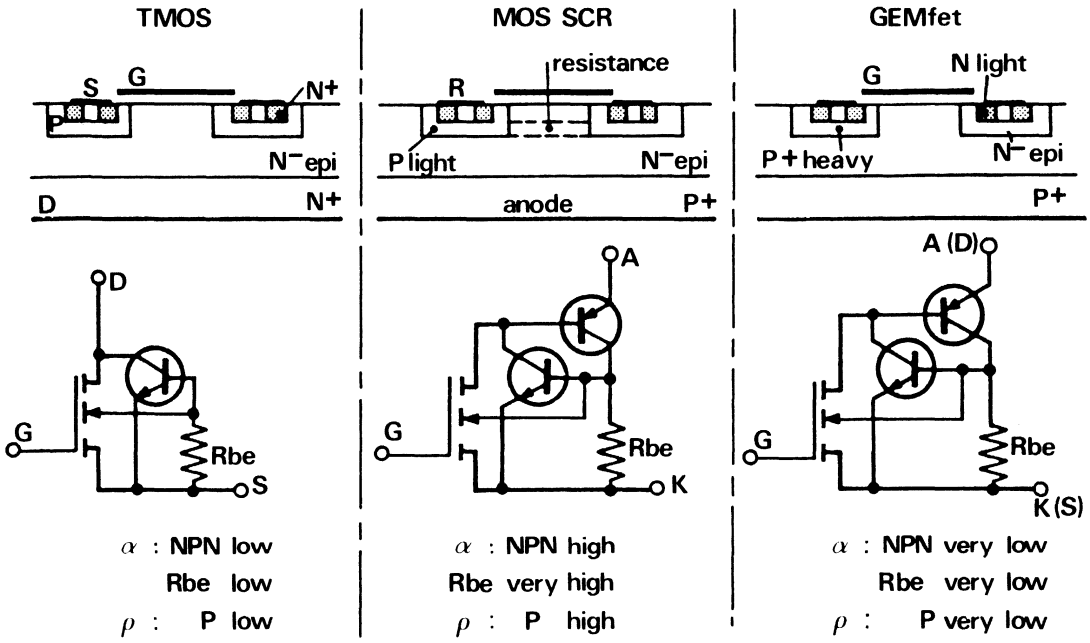


Figure 2-131

Identical structures are now produced by General Electric: IGT, insulated gate transistor and RCA: COMfet conductivity modulated fet.

The symbol for the GEMfet is defined as shown. It represents a normal Fet with input gate, source, and drain. The drain, however, has an arrow head which represents the emitter-base junction or rectifier of the PNP bipolar transistor.

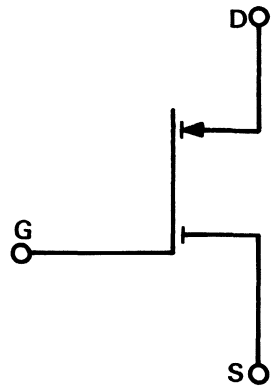


Figure 2-139

We can also note that thanks to layer P+, the freewheeling parasitic diode no longer exists for this type of product. In some applications this is good but in others the need to add an ultrafast rectifier external is a troublesome cost adder.

B) Electrical characteristics

B-1. Static characteristics: $I_D = F(V_{ds}, V_{gs})$

For better comparison of the advantages of the 3 structures, let us take 3 products with the same silicon die area: 16 mm², the TMOS MTP4N50, the MOS SCR MCR1000 and the GEMfet MGP20N50.

We can see immediately from the 3 characteristics areas that we have:

- Ron TMOS ≅ 1.2 Ω
- Ron. eq. MOS SCR ≅ 0.032 Ω
- Ron eq. Gemfet ≅ 0.16 Ω

We can already say that the GEMfet has an Rdson equivalent in surface unity 7 to 8 times less than the equivalent TMOS.

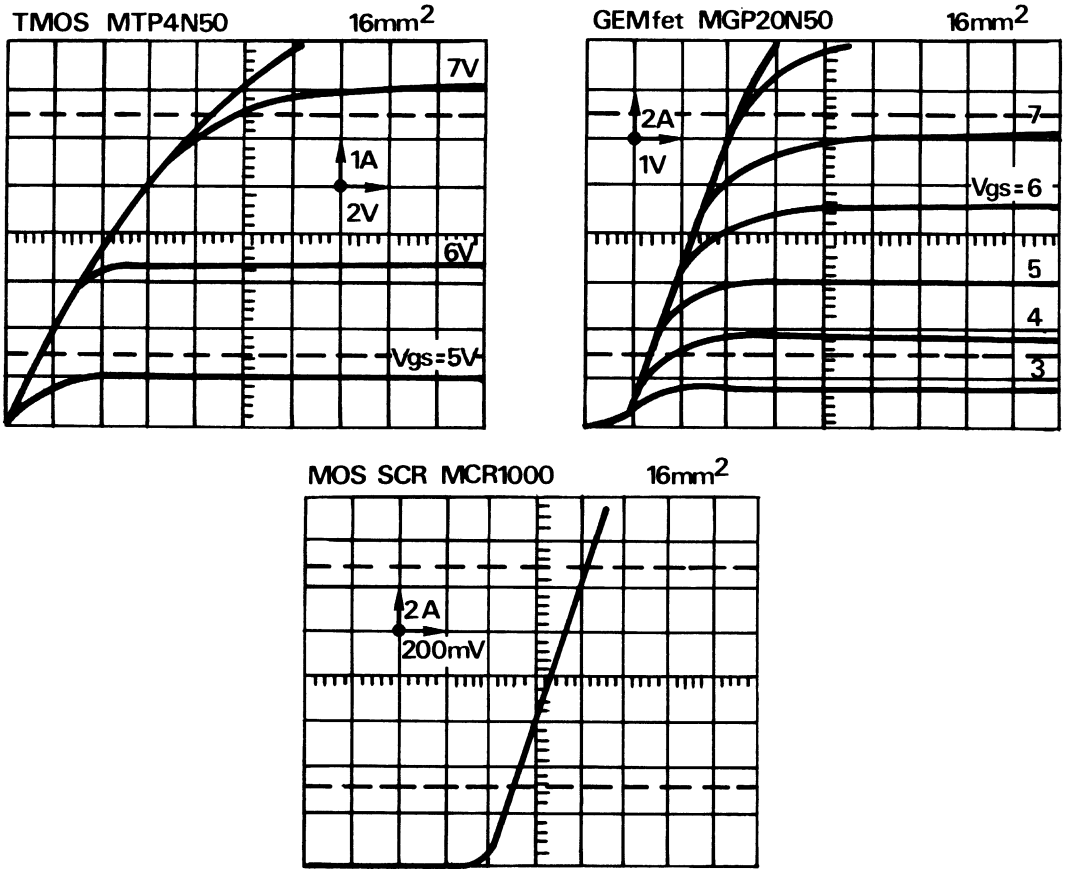


Figure 2-133

We can also see that the GEMfet has a minimum voltage drop offset of 0.6 V like an ordinary SCR or a MOS SCR which the ordinary TMOS does not have. This offset is due to the rectifier equivalent of the PNP base emitter junction. As such this can make

GEMfets undesirable for low voltage applications because of the additional power loss.
Comparing dynamic operation losses for these products again with a Darlington of equivalent surface (16 mm²), the BU522, we obtain Figure 2-134.

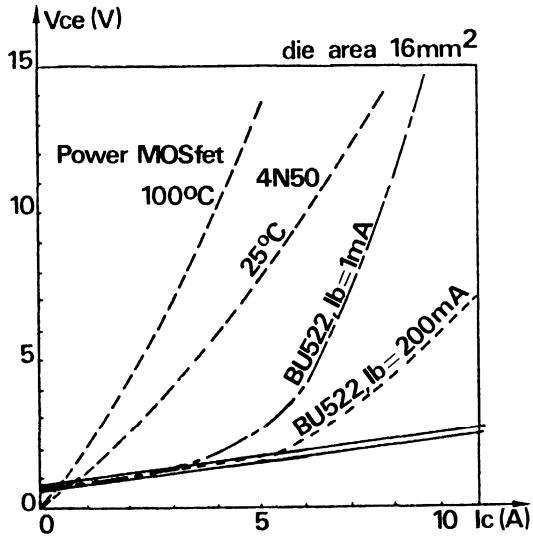


Figure 2-134

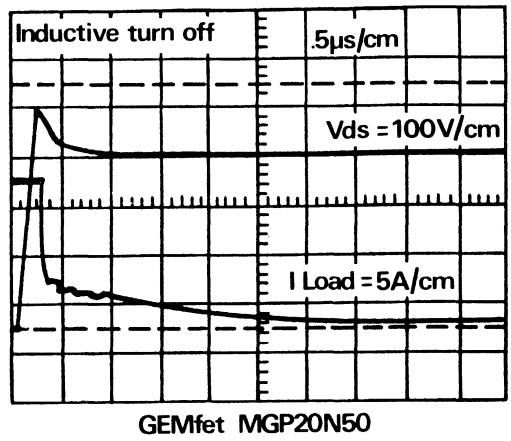


Figure 2-135

As shown in Figure 2-134, the GEMfet compares favorably with the bipolar transistor in terms of losses at room and extended temperature.

B-2. Switching times

The turn on times for a GEMfet as well as the TMOS power fet or the MOS SCR, are all very good: about 50 ns with a VGS peak of 15 V.

Unfortunately, due to the fact that there are minority carriers injected into the epi region of the structurte, these must recombine when VGS gate voltage is removed. This turn off time is thus relatively long: 3 to 4 microseconds.

As shown in Figure 2-135, there is first of all a severe drop in current then a long extended time for recombination.

Nevertheless this extended current tail can be improved by using the usual techniques of killing carrier lifetimes: heavy metals, irradiation.

If the various switches are compared in terms of total losses in relation to operating frequency, the results would be as shown in Figure 2-136.

On this curve, for present-day products, the GEMfet only competes with the MOSfet or the bipolars up to about 1 KHz.

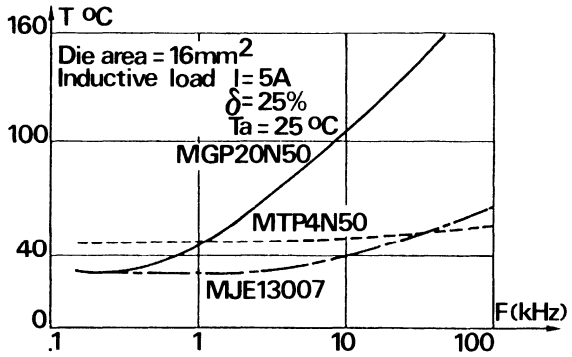


Figure 2-136

B-3. Safety areas

B-3.1. FORWARD BIAS SAFE OPERATING AREA: FBSOA

Figure 2-137, shows on one graph the forward bias safe operating area of the GEMfet MGP20N50 and that of the TMOS MTP4N50.

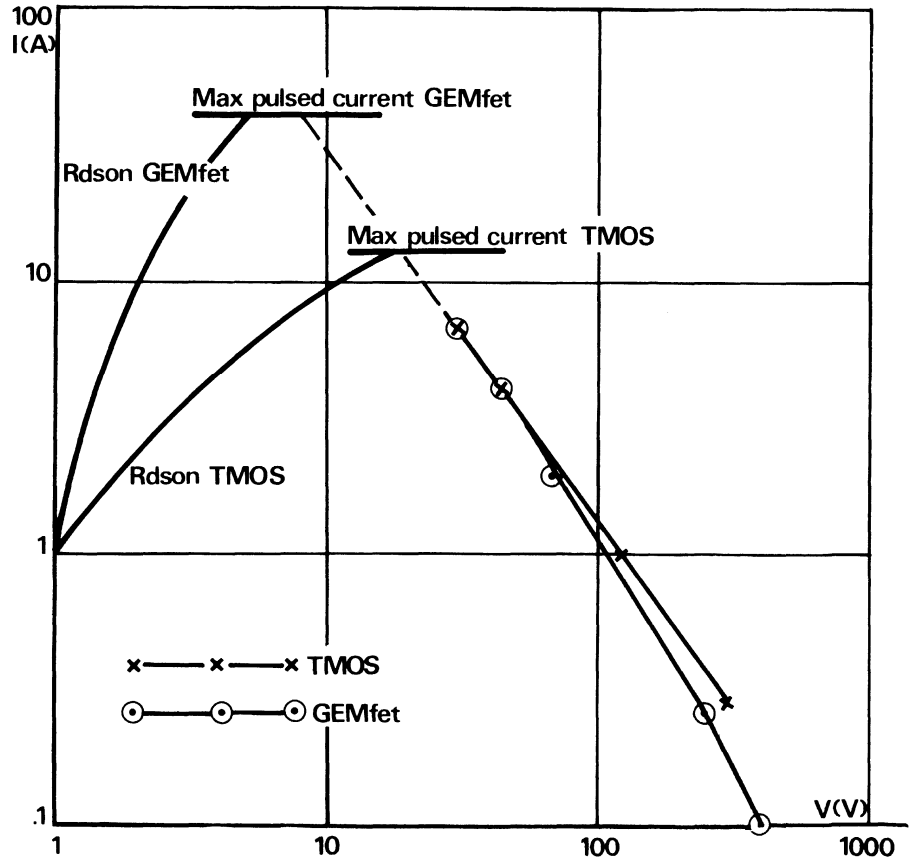


Figure 2-137

Notice straight away that the GEMfet has a smaller safe area than the TMOS equivalent in high voltage. This is not surprising as it is a Darlington with bipolar PNP.

At low voltage, on the contrary, thanks to better Rdson and better silicon efficiency, better possibilities exist in current limits.

B-3.2. REVERSE BIAS SAFE OPERATING AREA: RBSOA

As for bipolars, this safe area is reduced when compared with that of the corresponding TMOS. It is also sensitive to temperature, and to gate drive.

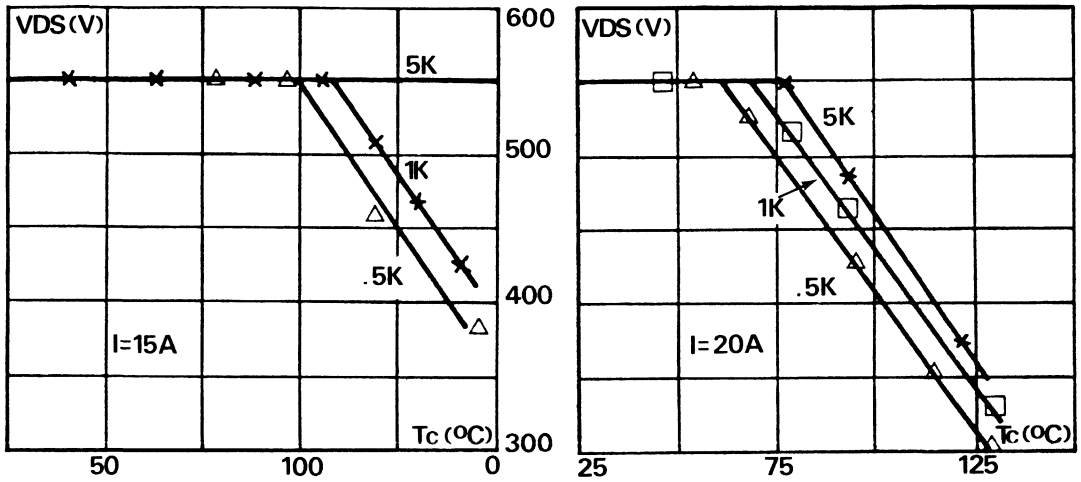


Figure 2-138

It can be seen that if the gate resistance is high, there is a better safe area in spite of the fact that the energy lost in switching is greater. This is perhaps due to high dV/dt applied to the PNP transistor of the darlington BIPMOS.

C) Applications

Initially the GEMfet will be limited to applications needing a solid switch, good overload capacity, with simple control and relatively slow switching times.

Two types of applications immediately emerge:

- control of a three phase motor of medium power (1kW)
- ignition switch for combustion engines.

We shall look quickly at the case of the ignition switch. Until now the triple diffused Darlington has been the only technology used which allows high energy to be supported at turn off.

The GEMfet can support this high turn off and in addition the low energy needed by the gate is equally desirable in the automobile.

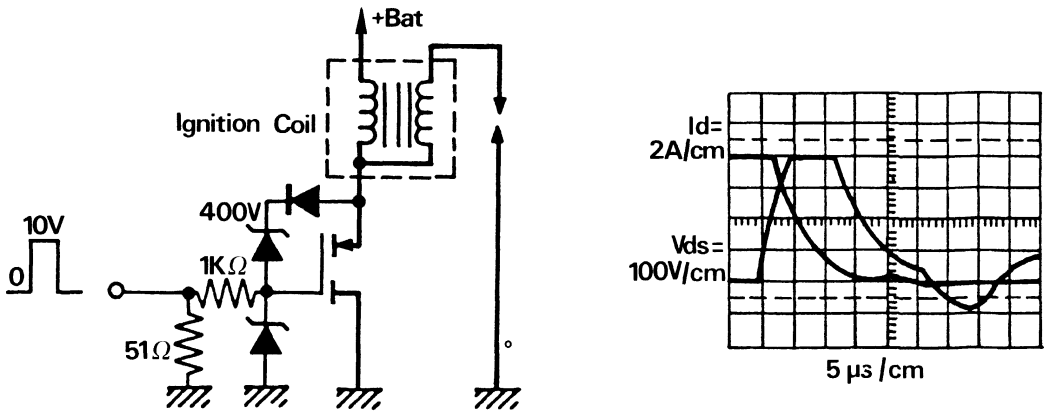


Figure 2-139

5. The Motorola power integrated circuit SMARTpower

A) Introduction

The ideal power switch does not exist, which is why designers of power applications have been trying for a decade to mitigate all the imperfections of semiconductor electronic switches. Applications often required sophisticated base drive circuitry as well as various forms of protection for overvoltage, over current and thermal stress. These additional networks heavily burden the total system cost of the assembly. This increase cost is due to additional design time, mounting and cost of components, and a compromise on system reliability.

The old dream of a automatic protected or blowout proof power switch and direct interface control by low level logic has still not been abandoned. The classic bipolar integrated circuit technology uses a horizontal transistor transistor structure and limits applications to the lower ampere current levels. The move towards higher power integrated circuits implies using a vertical structure to make a more efficient use of silicon.

This semiconductor concept, requires using advanced power transistor technologies and at the same time integrating small signal circuit techniques from integrated circuit technologies. This is the reason why at Motorola the SMARTpower team comes under the responsibility of the power products division. The CAD design computers developing this concept are linked with all Motorola computers using the integrated circuit concept. Design and processes are total compatible with the bipolar integrated circuit group.

B) Technology

To begin with, the significance of the word SMARTpower already gives us a good idea of the goal in mind.

This technology means that from now on epitaxial or triple diffused bipolar devices can be integrated on the same substrate along with power MOS and bipolar logic, CMOS, ECL, Schottky, with an integration density of more than 100 elements on the same chip.

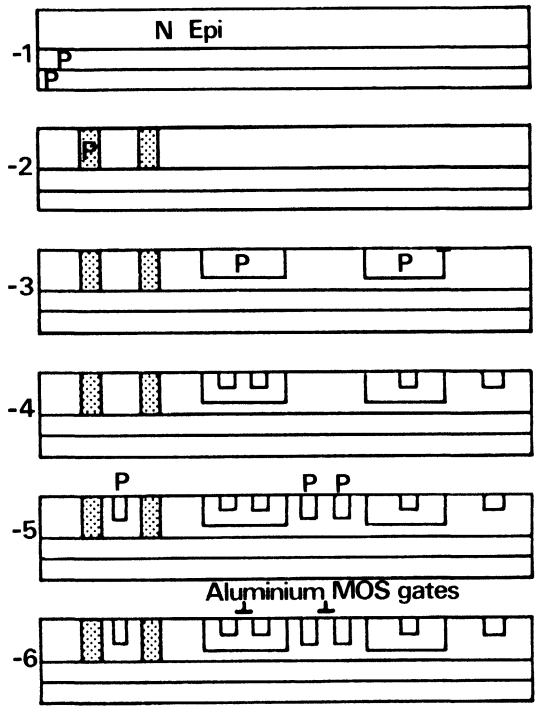


Figure 2-140 – SMARTpower diffusion stages

In Figure 2-140, we can see the different diffusion stages for the common elements for logic or power (five masks). For example, the diffusion of P+ for the power PNP bipolar emitter is performed at the same time as the Source and Drain of CMOS P channel transistor. This demonstrates the economy of the SMARTpower diffusion process.

Figure 2-141 and 2-142, show two possibilities among others for the output of a SMARTpower product: either a bipolar PNP or an N- channel power MOS.

The geometry used for either the bipolar power product or the Power MOS is a very fine technology and is identical for both types of technology. The cells are of dimensions less than 20 microns with width metallizations less than 10 microns and channel lengths of a few microns.

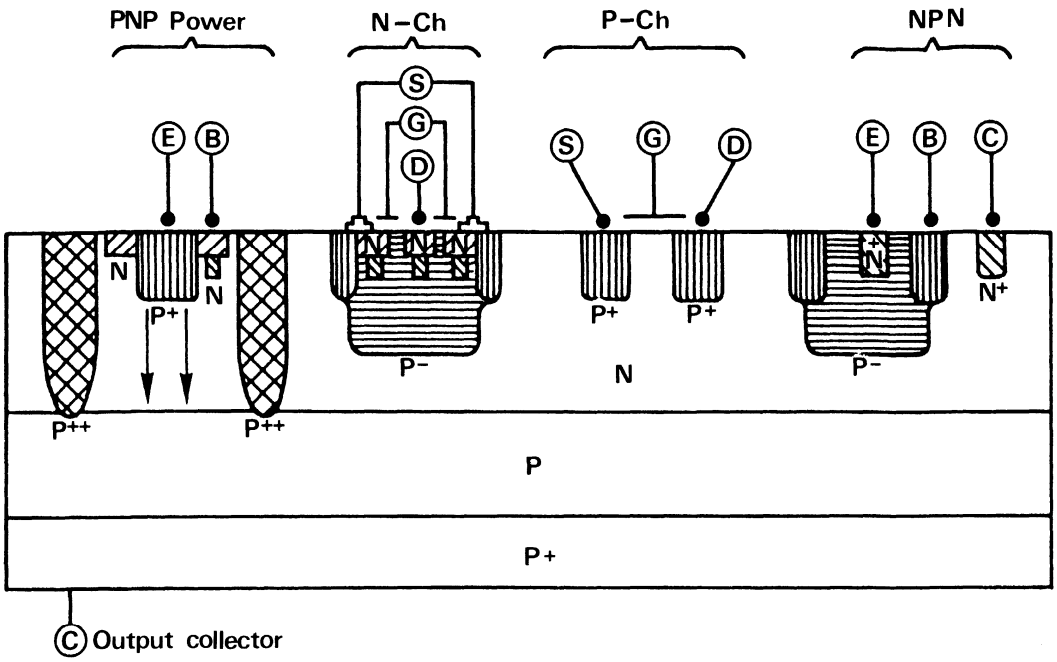


Figure 2-141 – SMARTpower vertical profile

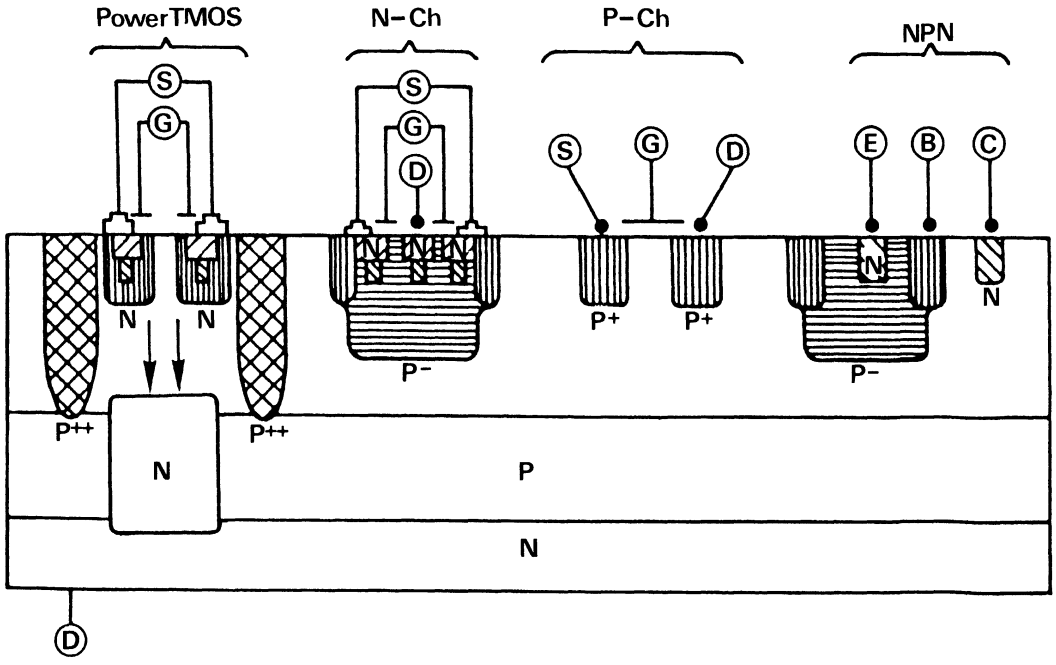


Figure 2-142 – SMARTpower II

Generally speaking, CMOS control logic is used as it is a reliable, well known technology capable of achieving the desired production results. It is useful in constructing numerous logical circuits such as parallel series coding and decoding, antisaturation circuits, protection circuits and drive interface.

It is equally compatible with either the bipolar or power MOS output process technology.

C) Series regulator

The first problem to solve in this technology where power is integrated with logic, is thermal dispersion. To demonstrate the mastery of this, Motorola constructed a series pass voltage regulator circuit with a 5V output at 10 Amps and 80 Watts, the MPC100, in TO3 case. The chip is shown in Figure 2-143.

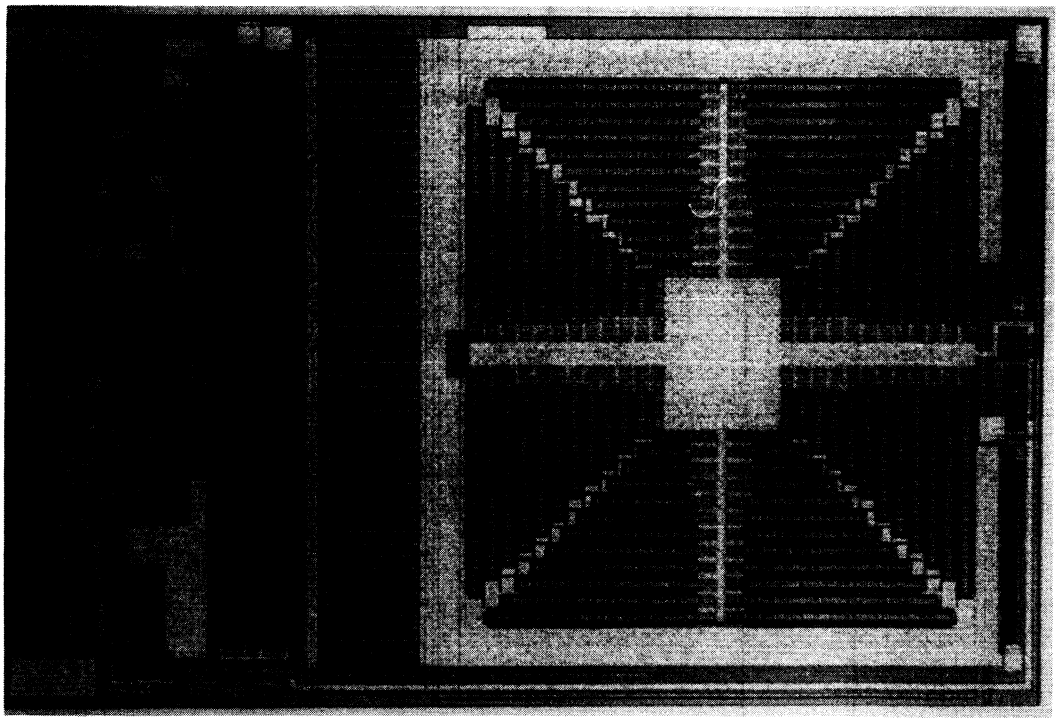


Figure 2-143 – SMARTpower, MPC100, chip (24 mm²)

The block diagram for the system's logic is shown in Figure 2-144, where the classic operations can be seen:

- reference voltage and current
- error amplifier
- different protections: thermal, maximum current, safe operating area

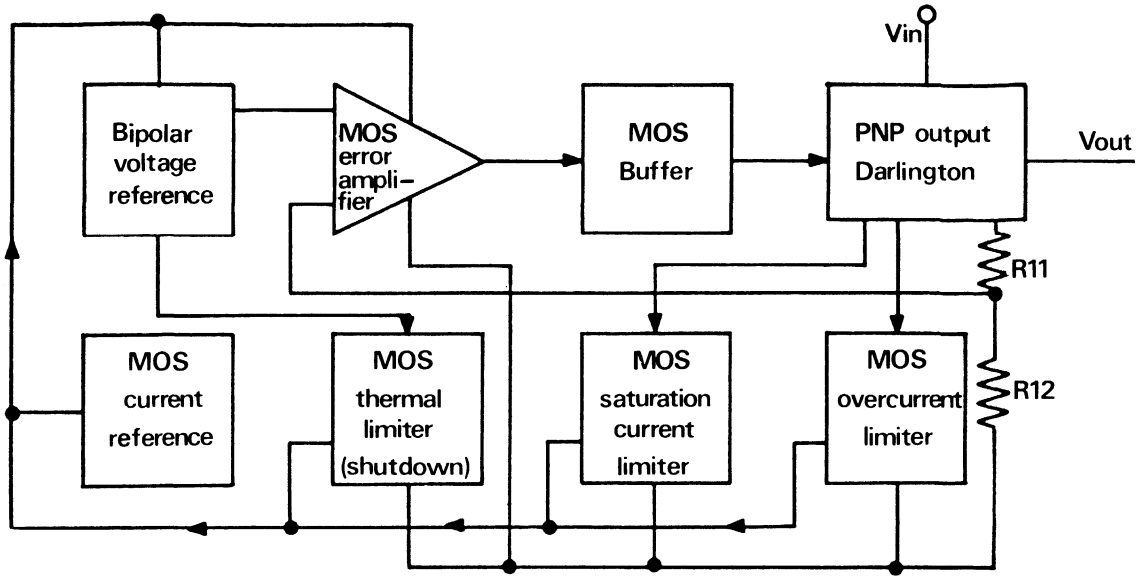


Figure 2-144 – SMARTpower, MPC100

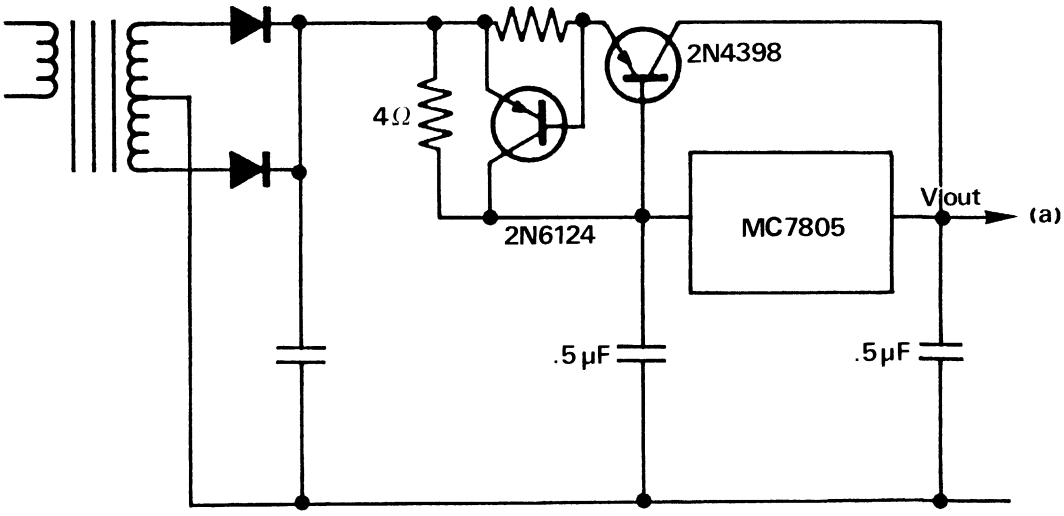


Figure 2-145 (a) – Typical regulator: MC7805 (I.5A-5V)

In Figure 2-145, an example is given where the economy introduced by this product is clearly demonstrated.

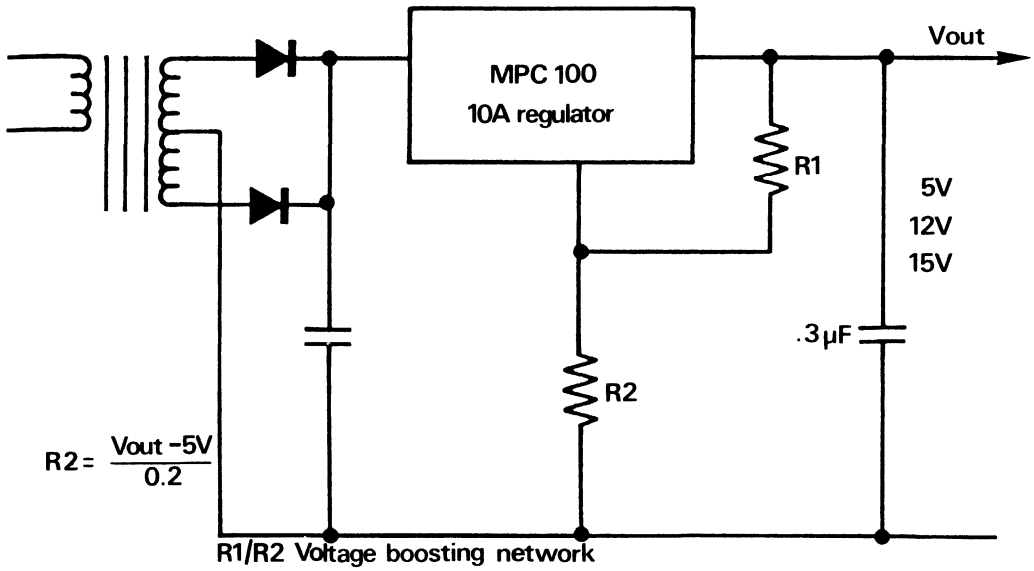


Figure 2-145b – SMARTpower, MPC100

D) Packaging

Figure 7: Future packages for SMARTpower

The first package used for the regulator is a metallic TO 3; it can also be a plastic TO 3 P but the increasing complexity of functions resulting from this technology necessitates a multi-leaded package.

A market research study revealed that the package in Figure 2-146, are the most often desired, so future SMARTpower products will begin to appear in a case of these types.

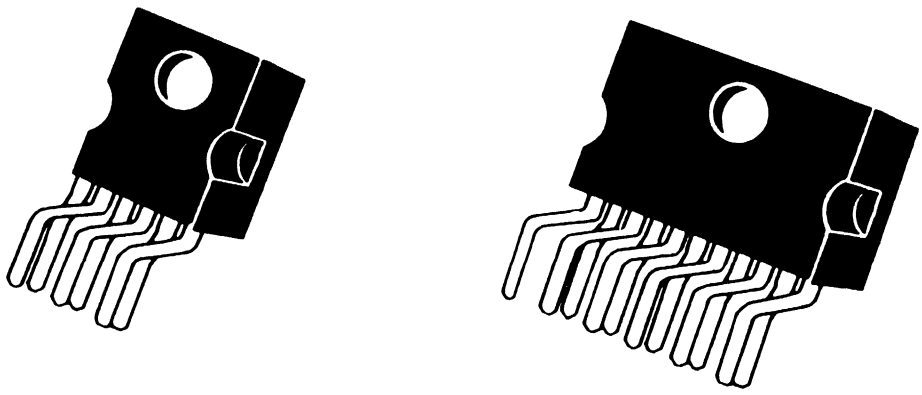


Figure 2-146 – SMARTpower, multi lead power package

E) SMARTpower program

For this technique, Motorola has already defined 3 production technology levels as shown in Figure 2-147.

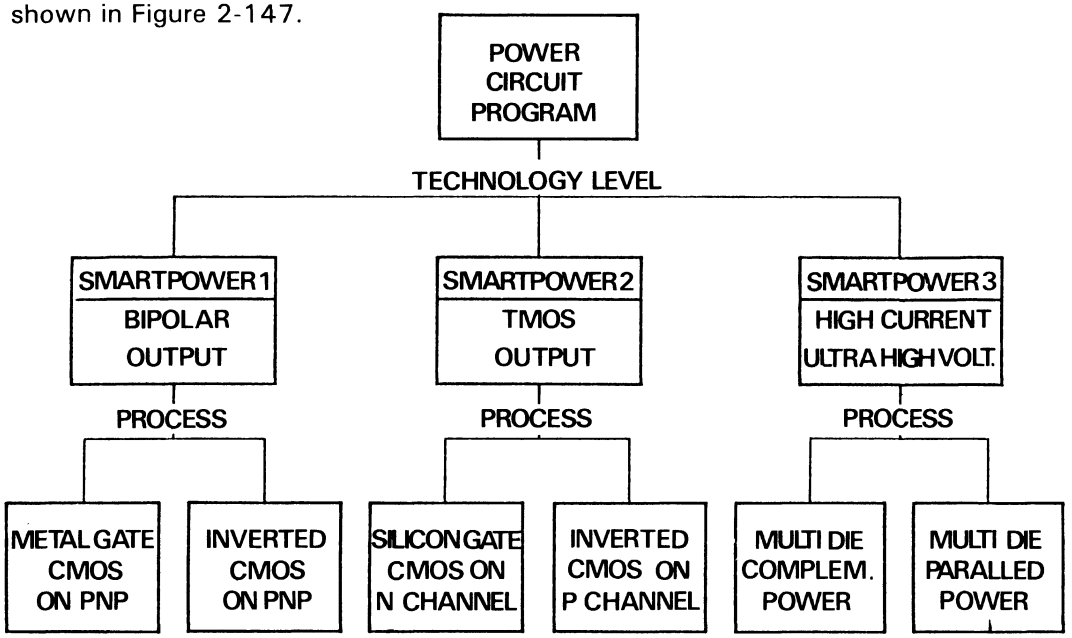


Figure 2-147 – Different SMARTpower technologies

The power which these different technology levels can control is shown in Figure 2-148.

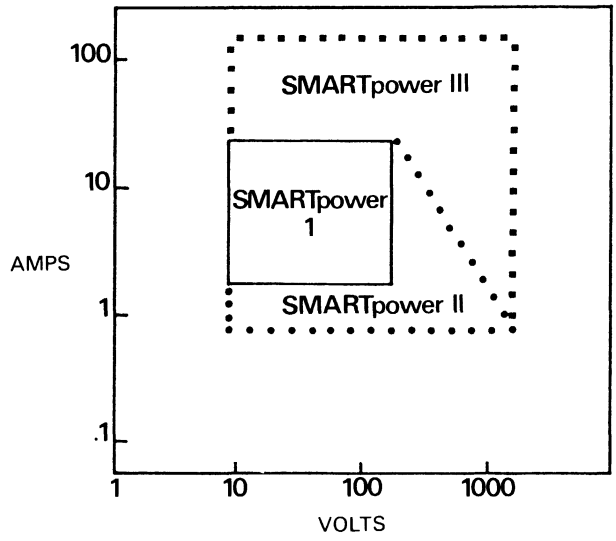


Figure 2-148 – Power possibilities of different SMARTpower technologies

We can see in this figure that if we have a switch application of 50A working on rectified 380 V (540 V continuous), it most likely would be made in SMARTpower III.

Possible future products

In the near future the range of series regulators will increase from 5V 10A to 15V 10A. Programmable zeners or voltage protectors may appear, with maximum current of 300 A and zener voltage from 6.2 V to 17.2 volts. Also the first products designed for the automobile (relay, switchmode, power supply, etc.).

Other prospective products

Having shown our "know-how" in terms of theory, the task now is to increase working voltage to demonstrate the feasibility of high voltage products in this technology.

E-1. Series regulators

Provisional short-term (1 year) increase the voltages to that of 100 to 200 V.

E-2. Programmable references

Power zener (Figure 2-149):

- for transient supressor circuits
- power references

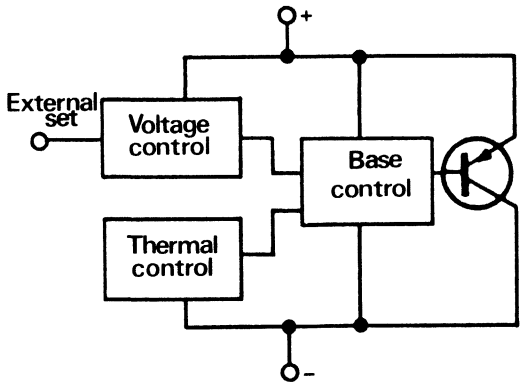


Figure 2-149 – Programmable power reference

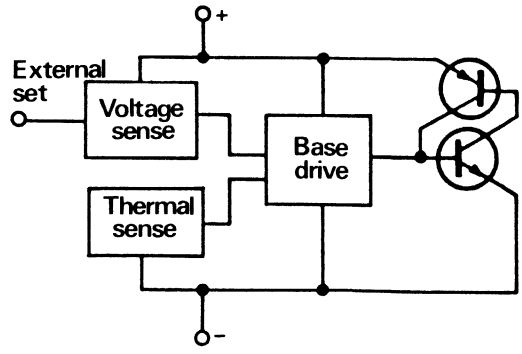


Figure 2-150 – Power pulse generator

E-3. Power pulse generators for: protection circuits ("crow bar") and flash generators, stroboscopes, etc... with maximum current of about 250 A (Figure 2-150).

E-4. Self protecting transistors

All power applications (Figure 2-151).

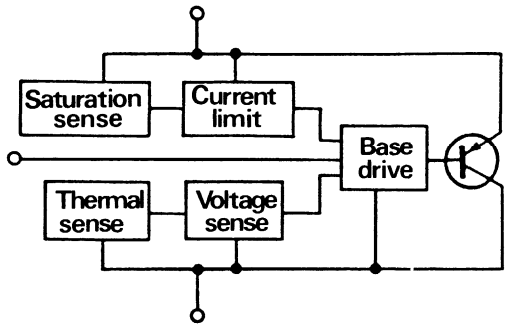


Figure 2-151 – Self protecting power transistors

E-5. Small motor controls:

- continuous current motor
- stepping motors
- polyphase motors

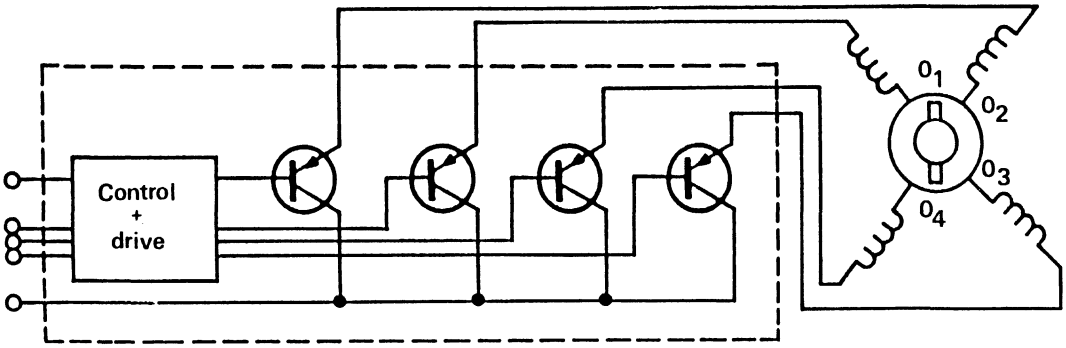


Figure 2-152 – Control of stepping motor

E-6. Logic controlled switches for:

- solenoïd control
- hammer driver control
- multiplex load control in automobiles

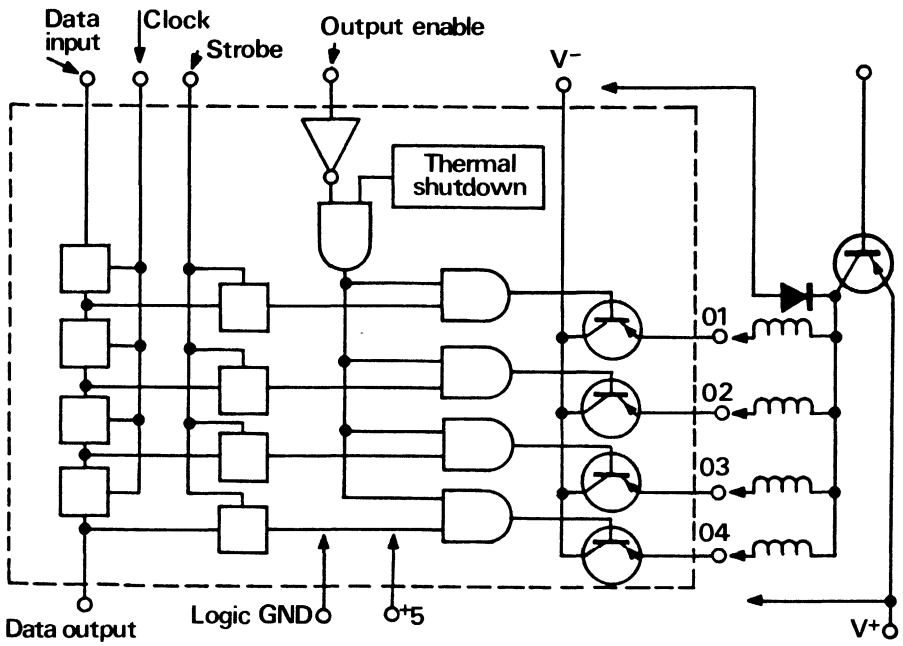


Figure 2-153 – Logic controlled switch

E-7. Switches in general

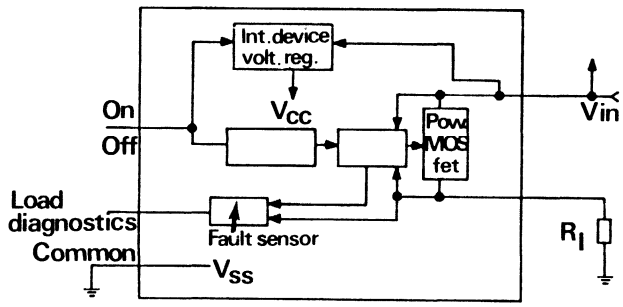


Figure 2-154 – SMARTpower, high side switch MPC1500

In Figure 2-154, it can be seen that a supplementary function has been added to this switch. The detection of a load fault or diagnostic for feedback to the control element (microprocessor).

One can imagine that following the detection of a load fault, not only may the switch be protected, but, and this is a far more important for the future of the system, it can now make a decision concerning the load itself:

- cancel the control
- diagnose the breakdown
- replace the load in the system with a spare load, or another identical load. For example, a car braklight is broken, the device can decide to light up a red rear light in its place.

E-8. Power switch for convertors as MPC1600

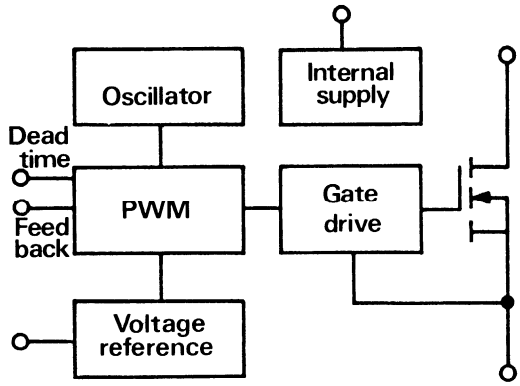


Figure 2-155 – PWM switch (pulse width modulation)

In Figure 2-155, we can see the possible integration of all the elements surrounding a power switch in a SWITCHMODE power supply. Clearly, in this list, automotive products will be the first candidates for SMARTpower technology, as they are not very high in voltage and they provide an enormous potential market.

F) Conclusion

If one looks to the year 1990, it will be certain that the power products used then will be very different from those of today. One of the development axes, for creator of power products, is obviously to put into the market products which are unbreakable and easy to control, at prices which allow power electronics to establish themselves mainly through cost reductions and very good reliability.

The SMARTpower technology is clearly a vehicle for tracing this migration path.

6. The thyristor

The name thyristor, given because of its analogy to the thyratron tube, is the generic name for a whole family of semiconductors having three or more junctions (four layers or more).

These devices, which can have two, three or four external terminals, are bistable (off and on) in operation and may be uni- or bi-directional.

A) Thyristor family

The best known member of this family is the SCR (silicon controlled rectifier), it is also known as a reverse blocking triode thyristor which is a unidirectional conducting device having 3 terminals (anode, cathode and gate).

Table 2-1, describes the low power thyristor trigger devices, showing their typical blocking voltage and operating current range. Not shown in this table is the Shockley diode, a two terminal, four layer trigger which has characteristics similar to the DIAC family of devices – negative resistance. The other listed triggers, be it the UJT, PUT, SUS, SBS or SCS, feature this characteristic of the triggers shown, the silicon controlled switch (SCS) is the only 4 leaded device and is therefore called a reverse blocking tetrode thyristor.

The bidirectional conducting DIAC has only two junctions but it performs in a manner similar to the four layer (3 junction) devices. The word diac, defined by GE, signifies Diode Alterning Current switch. Products set off, by light, LAPUT, LAS, LASCR, LASCS have not been shown but they have the same characteristics as the listed devices

Table 2-1 – Thyristor (I)

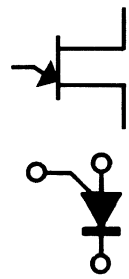
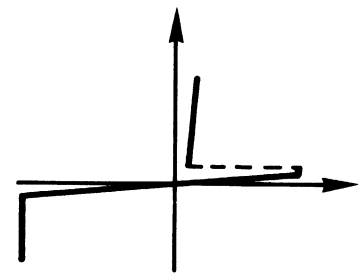
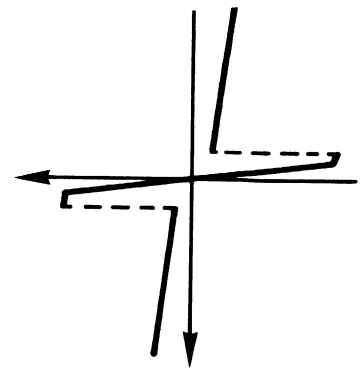
UJT PUT	Unijunction transistor 40 V – 100 mA Programmable unijunction trans. 40 V – 15 A		
DIAC	Bidirectional trigger DIAC NPN 50 V – 10 mA		
	Bidirectional diode thyristor 50 V – 100 mA		
BILATERAL	Sidac 180 V – 1 A		

Table 2-2, shows the power thyristor family.

The GTO (gate turn off) is also called GCO (gate cut off), gate controlled switch (GCS) or latching power transistor.

Included in this classification is the UJT (unijunction transistor) which is a special device with resistance variation by diode injection (unijunction) and whose operation is similar to that of the PUT.

Table 2-1 – (continued)

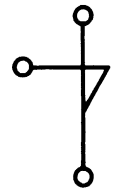
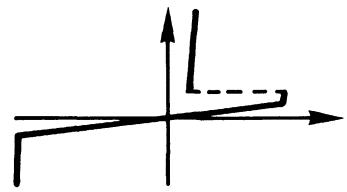
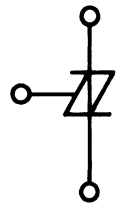
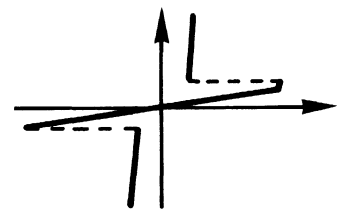
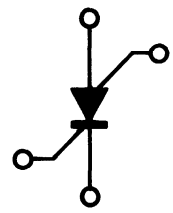
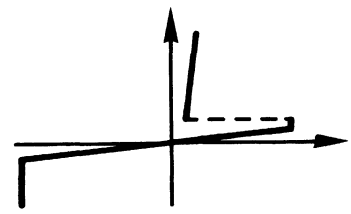
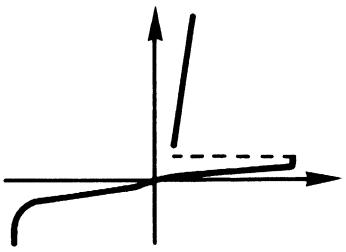
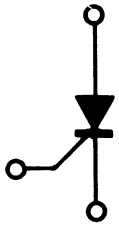
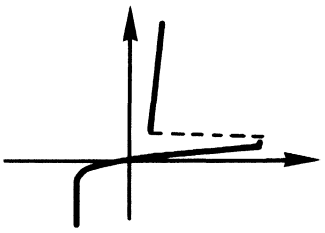
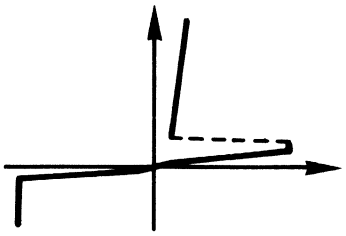
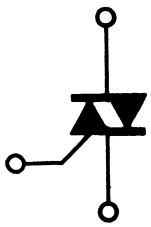
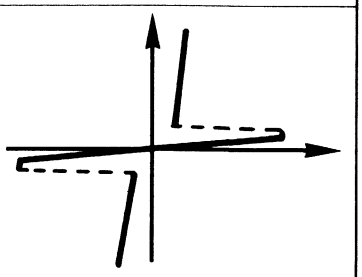
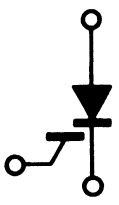
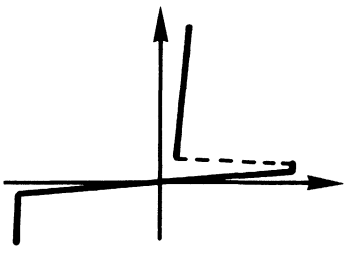
SUS	Silicon unilateral switch 30 V – 1 A		
SBS BILATERAL	Silicon bilateral switch 30 V – 1 A		
SCS	Silicon controlled switch 100 V – 1 A		

Table 2-2 – Thyristor (II)

SCR	Silicon controlled rectifier 4 KV – 4 KA		
ASCR	Asymmetrical silicon controlled rectifier 2 KV – 1,5 KA		
GTO	Gate turn off 4 KV – 2 KA		
TRIAC	Triode AC switch 600 V – 40 A		
MOS Thy	MOS thyristor 500 V – 20 A		

B) SCR Working

B-1. Basic equations

An SCR is a device with 4 layers and 3 junctions having 3 external connections: anode, cathode and gate. It is a bi-stable product on - off.

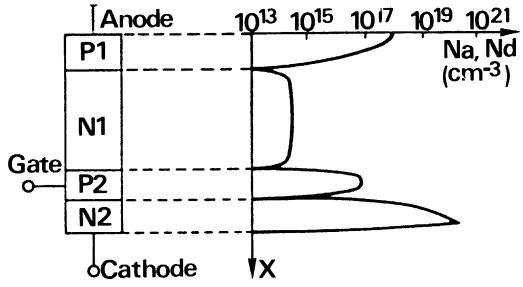


Figure 2-156 – The SCR with its doping profile

2 transistors model describes the SCR operation.

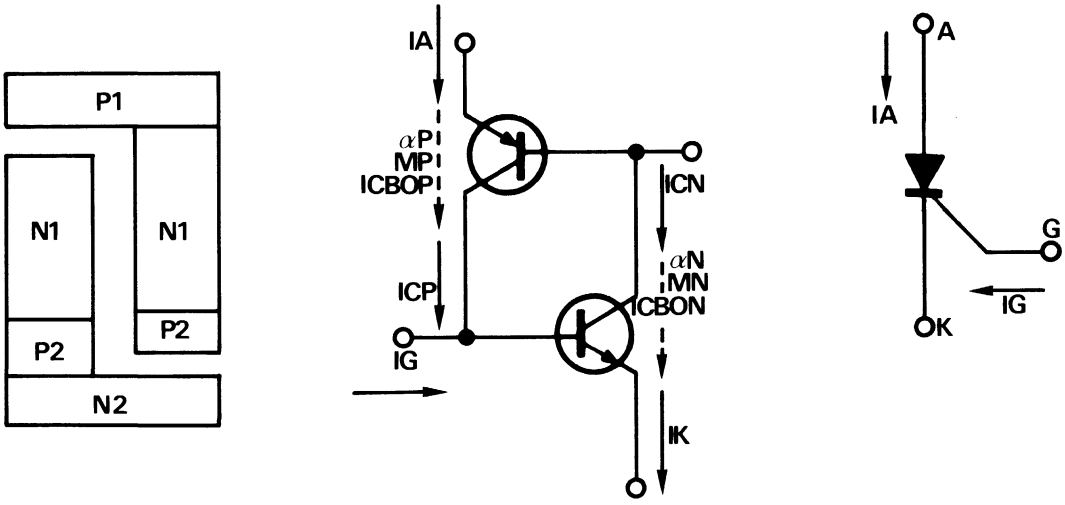


Figure 2-157 – SCR analogy

May be written as: $I_{CP} = \alpha_P I_A M_P + I_{CBOP}$ and $I_{CN} = \alpha_N I_K M_N + I_{CBON}$ with $M = \frac{1}{1-(V/VB)^n}$: Miller's equation.

VB = avalanche voltage, n = 4 for NPN and 2 for PNP. Also (Kirchoff's law).

$I_G = I_K - I_A$ and $I_A = I_{CP} + I_{CN}$ hence $I_A = \alpha_P I_A M_P + I_{CBOP} + M_N \alpha_N (I_G + I_A) + I_{CBON}$-, $I_A (1 - \alpha_P M_P - \alpha_N M_N) = \alpha_N M_N I_G + I_{CBOP} + I_{CBON}$-

$$I_A = \frac{\alpha_N M_N I_G + I_{CBOP} + I_{CBON}}{1-(\alpha_P M_P + \alpha_N M_N)}$$

It can be shown that at ambient temperature and for VA < VB supply MP ≅ MN ≅ 1. The main question remains then how to vary the common base gains for αN and αP composite transistors, as function of current or current density J.

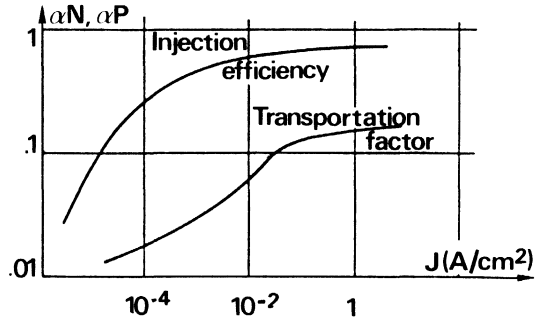


Figure 2-158 – Variation of αN, αP = f(J)

Also αP increases with VAK supply voltage due to the EARLY effect

Therefore at ambient temperature and for VAK < VB.

$$IA \cong \frac{\alpha N\, IG + ICBOP + IBON}{1 - (\alpha P + \alpha N)}$$

Without IG, currents are very small at αN ≅ αP ≅ 0, resulting in: IA ≅ ICBOP + IBON (leakage currents).

B-2. Triggering

To trigger the device, the loop gain G = αP MP + αN MN should approach unity resulting in several solutions:

B-2.1. By increase VAK to VB, MP and MN increases and G approaches 1.

This is the working mode for 4 layers diodes.

B-2.2. Temperature: leakage currents in silicon doubles roughly every 8°C. If these currents rise sufficiently high, IA will increase causing αN and αP to increase and the device will trigger on.

B-2.3. Light: An incidental light energy e = hν, may, if high enough, create pairs of electron holes, thus increasing the leakage currents and triggering the device.

B-2.4. The rate of change of the applied voltage supply: dVA/dt in forward mode (VAK > 0).

The center junction N1-P2 alone supports this potential.

If the rate of voltage is fast enough, a current will be induced into the base of the NPN transistor equivalent to ib = C dV/dt causing the device to trigger on (fire).

B-2.5. The most common method for on triggering the SCR, is to turn on the base of the NPN transistor.

αN increases with IG, G approaches 1, and the SCR fires.The PNP transistor base can also be used.

Example: An SCS which has 2 bases, but αP is always less than αN and thus more energy would be needed to turn on the structure.

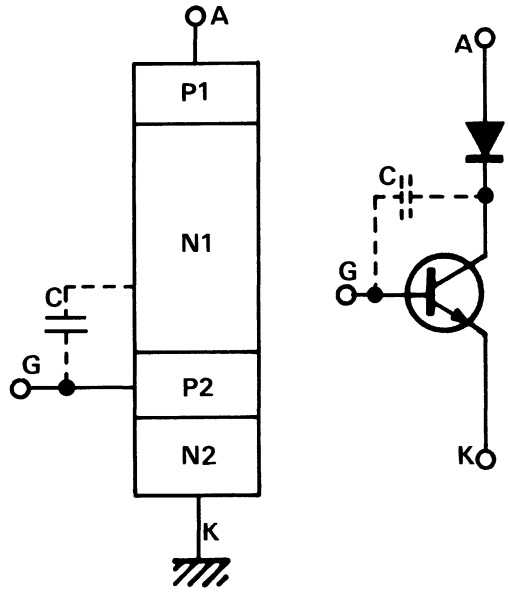


Figure 2-159

B-3. Diagrams of internal state of SCR

B-3.1. STABLE STATE WITHOUT POLARIZATIONS: Figure 2-160

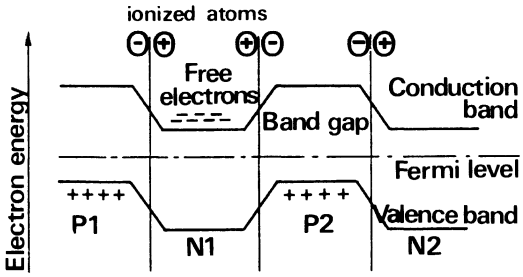


Figure 2-160 – Diagram of SCR

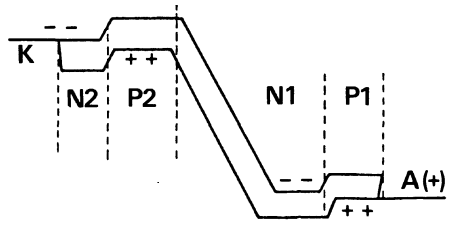


Figure 2-161 – Blocking state with positive supply VAK > 0

B-3.2. PASSAGE FROM STABLE STATE TO BLOCKING STATE WITH A POSITIVE SUPPLY

Using a positive supply without gate control (VAK > 0) resulting Figure 2-161

The shape of the band gap is more deformed in the lightly doped region (region N1) and becomes the high depletion region: the electrons attach to their low energy regions (low regions) and the holes also attach to their low energy regions (high regions). These carriers cannot cross the depleted region as they have too little energy . (≅ 1.12 e. Volt) to get through junctions N2 P2 and N1 P1.

B-3.3. PASSAGE TO CONDUCTION STATE: Figure 2-162

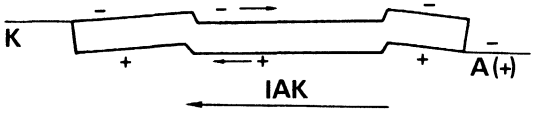


Figure 2-162 – Conduction state

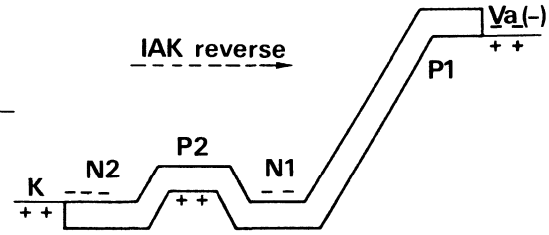


Figure 2-163 – Reverse blockage

When a positive Vgk voltage is applied to the gate, the energy of its electrons (P2) is reduced and the potential level lowers enough to allow the emitted electrons to get through the depleted region, due to the electric field. These electrons, at the base of junction N1, increase its potential level. The increase of carriers in all junction collapses the potential barriers and current IAK is now only limited by the network external to SCR. The VGK potential to device cause conduction is approximately 0.8V.

B-3.4. PASSAGE TO BLOCKED STATE

The passage to blocked state is brought about by reverse voltage.

When we apply VAK reverse voltage, the anode potential is such that the energy diagram becomes as shown in the Figure 2-163.

The junction N2-P2 (gate-cathode) potential barrier is blocking first between two highly doped regions, which allows fast recombination of excess carriers brought by conduction.

Following this junction P1 N1 potential barrier reforms itself followed by that of central junction N1 P2, until this moment VAK voltage stays roughly equal to 0.7 V.

The disappearance of excess carriers is accelerated by the appearance of the potential barriers and the reverse current: the N1 depleted region appears. If required the product can revert to its direct blocked state without any problem.

If the blockage was brought about simply by disappearance of VAK, it would take a long time for excess carriers brought by conduction to disappear and a positive VAK voltage could only be reapplied after leaving the SCR blocked for a fairly long time: between

several microseconds and several hundreds of microseconds depending on the technology and the power of the product. The time taken between direct current turn off and the moment when direct voltage can again be applied without risk of reconduction is called "turn off time" or tq.

C) I-V characteristic of SCR

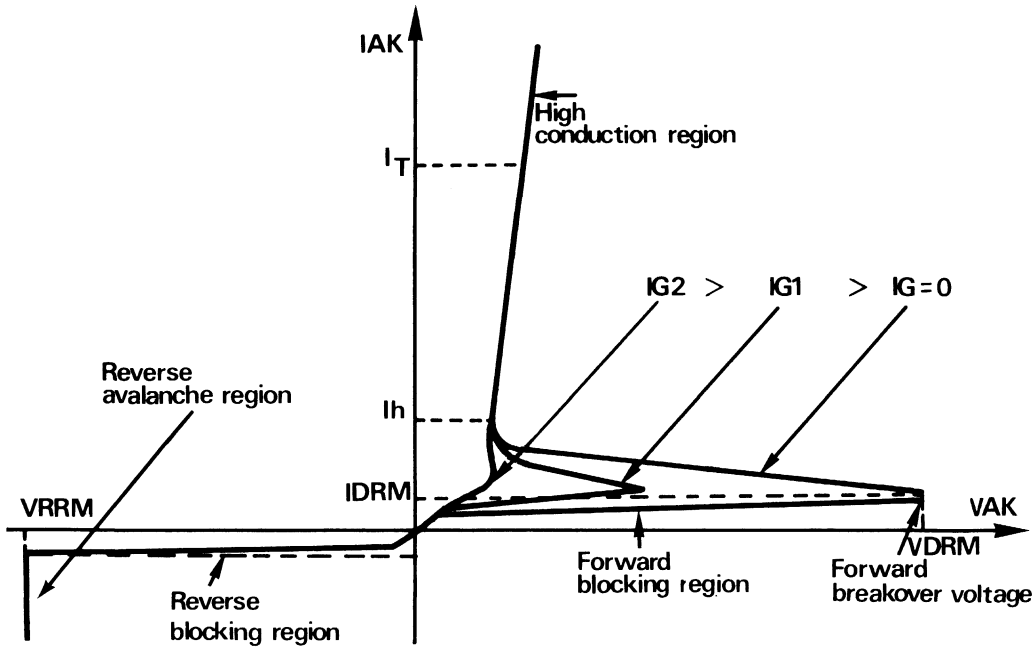


Figure 2-164 – I-V characteristic of SCR

In the forward blocking region, leakage current increased until the avalanche (VBO) yields a loop gain > 1 and turns on the SCR, resulting in low impedance.

For reverse polarity, the device appears as a reverse biased diode until the breakover point. For classic structures, SCR, SCS, LASCR, this reverse breakover voltage VRRM is greater than the forward breakover voltage VDRM or VBO. For normal operation, the SCR is supplied well below VDRM and firing is controlled by current injection to the gate (or light for the LASCR). When the load circuit allows a current greater than the latching current IL, gate control can be bypassed.

To block the device, the current must be reduced below a minimum current known as holding current Ih . The latching current obviously depends on the gate pulse conditions (Figure 2-165).

Temperature effects

The plane junction theory estimates that a rise in temperature increases breakover voltages VDRM and VRRM, on conditions to avoid junction N1-P2 junction N1-P2 leakage currents flowing to the gate: gate in short circuit or with a weak resistance with the cathode.

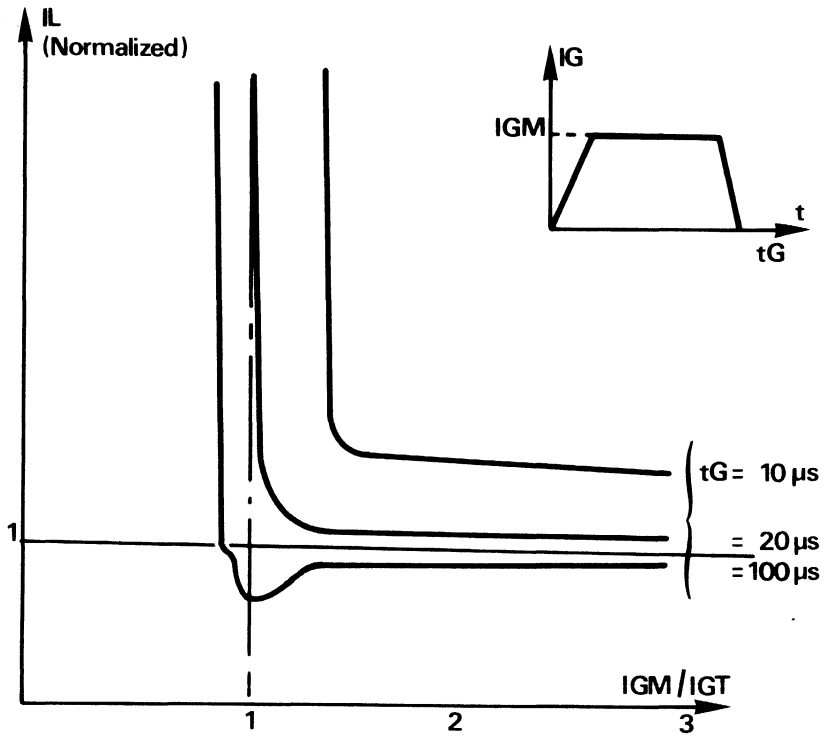


Figure 2-165 – Pulse control conditions

D) Gate control

D-1. Gate characteristics

The gate structure of an SCR can be considered to be a diode in series with a resistance, resulting in Figure 2-166, curve of gate characteristic.

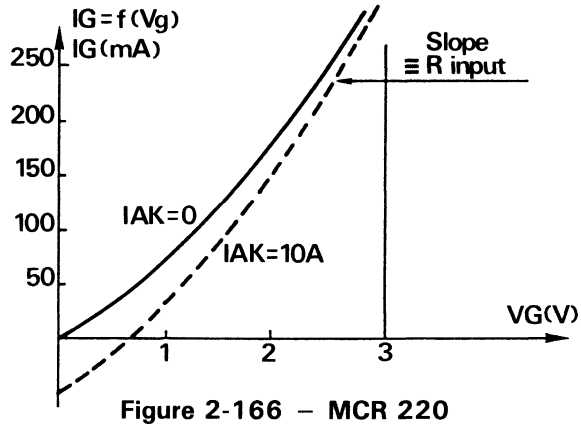


Figure 2-166 – MCR 220

D-2. Firing conditions

Figure 2-167, describes the gate load line drawn on the gate characteristic curves. The operating point, and its variation with temperature, should be well below the Pgm rating of the device.

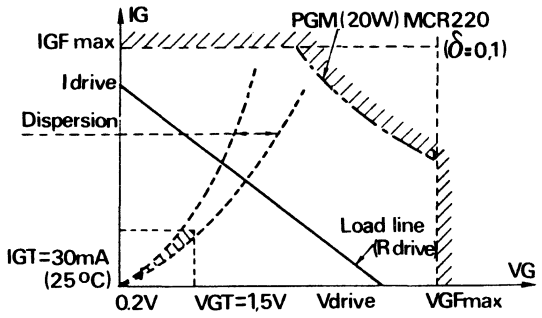


Figure 2-167 – Gate loadline

When using direct current for gate control Pg (AV) must not be exceeded. To ensure SCR triggering, adequate gate current must be supplied the gate must be controlled by pulse width, t, for a repetition period T and duty cycle δ = t/T where Pg (AV) = Pg max δ.

In any case, pulse width t, should be large enough to reach the trigger current. For inductive loads, t will be greater than for resistive loads.

D-3. Gate polarisations

D-3.1. The gate should not be forward biased when the SCR anode goes negative.

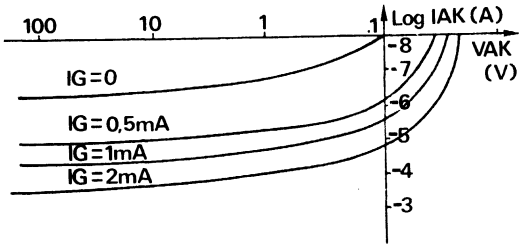


Figure 2-168 – IAK = F (VAK)

Under these conditions, the leakage current increases, as shown in Figure 2-168, resulting in increased device power dissipation. When Vgk < 0.25 V, this increased dissipation condition is eliminated.

If the SCR gate is forward biased (pulsed or D.C.) when the anode is negative, the additional temperature rise due to increased device dissipation should considered.

D-3.2. The gate can be negatively biased, whereby a reverse gate current flows, this reduces carriers available in gate zone P and thus allows increased blocking voltage capability up to the avalanche voltage at the center junction. This negative bias also has other advantages which will be discussed later.

D-3.3. To minimize pulse triggering of the SCR due to leakage current Igl, a small value of resistance Rgk, should be placed between the gate cathode. Thus, Vgk = Rgk Igl should be less than that value of Vgk to trigger the SCR.

D-3.4. Special case: opening of cathode circuit while operating. For thus condition, the load current circulates in the gate and is only limited by the circuit impedance. This may cause failure of the control network or the SCR itself.

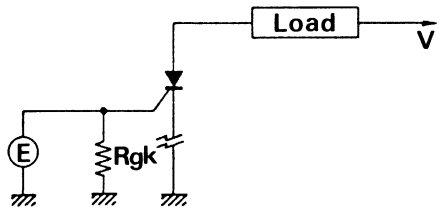


Figure 2-169 – Cathode/ground opening

E) Dynamic characteristics

E-1. Turn on

E-1.1. GATE CHARACTERISTICS

When a control pulse is applied to the gate, the voltage at SCR anode starts to decrease at the end of a certain time Td (Figure 2-170).

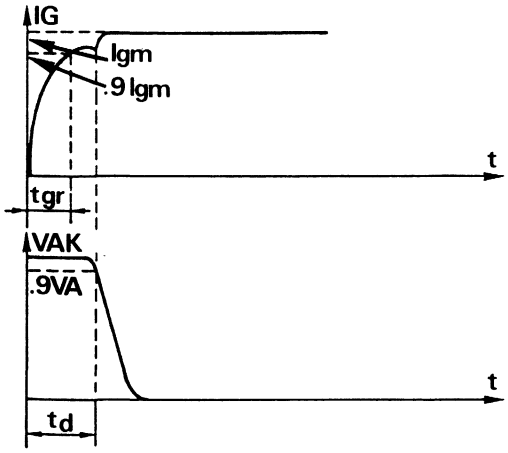


Figure 2-170 – VAK = f(IA)/t

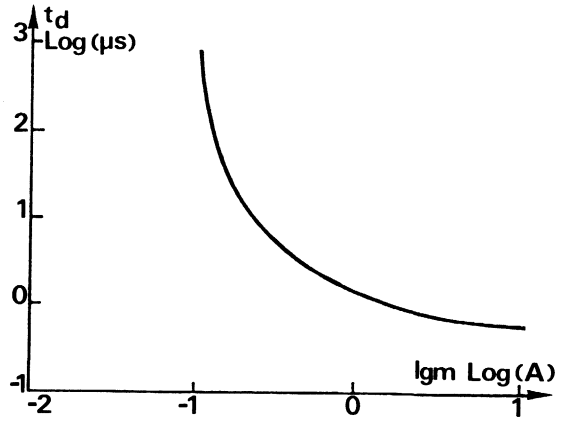


Figure 2-171 – td = f(Igm)

This delay time td is determined by the Igm value Figure 2-171 and rise time tgr of the gate pulse.

From these curves, it is clear that td can be reduced by increasing Igm, or by making. tgr as small as possible Figure 2-172.

From an empirical point of view the best compromise is: Igm ≅ 5 Igt. td has been defined to the 10% decrease point of VAK, this does not mean that from this point the structure is entirely conductive. In effect at the end of time td, only the surface of the chip next to the gate is conductive, from which conduction spreads throughout the silicon at a rate of approximately 100 $\mu m/\mu s$ (rate of plasma displacement). This variation of conduction time is illustrated in Figure 2-173.

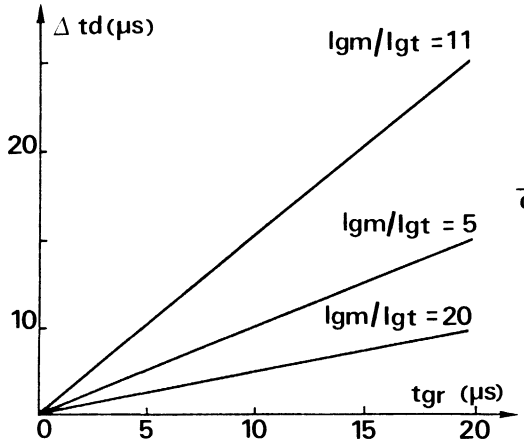


Figure 2-172 – $\Delta TD = f(tgr)/Igm/Igt$

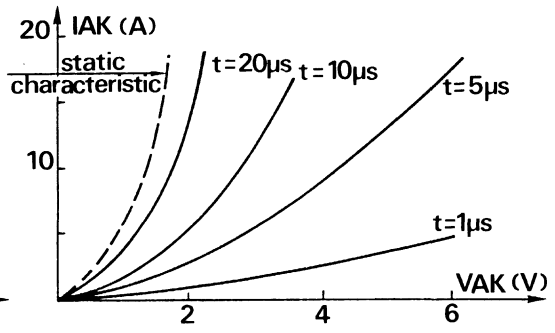


Figure 2-173 – Triggering of an SCR as a function of time

The triggering losses for a fairly high current (resistive load) can thus be very considerable, as shown by the figure 2-174).

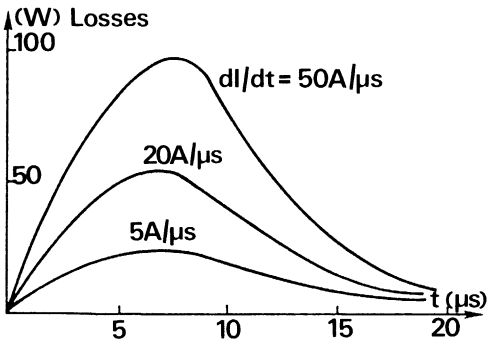


Figure 2-174 – Losses = f(dI/dt)

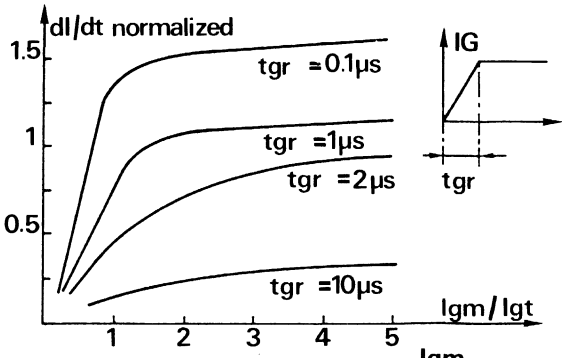


Figure 2-175 – $dI/dt = f\left(\frac{Igm}{Igt}\right)/tgr$

For each type of SCR, it is essential to define a critical limit of admissible dI/dt.

However this critical limit is given for conditions very specific to the state of the device before control and of control itself. Figure 2-175, shows the variation of dI/dt versus control variables.

E-1.2. PROTECTION AGAINST HIGH dI/DT

E-1.2.1. From the die design point of view: allow the highest possible dI/dt. The first thyristor chips had eccentric gate (Figure 2-176). Clearly, this geometry does not allow fast conduction of the structure; it seems obvious that a center gate is better (Figure 2-177). This structure can now be further improved by introducing interdigitated gates (Figure 2-178) set in a spiral (Figure 2-179).

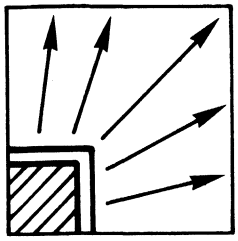


Figure 2-176

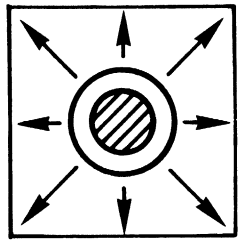


Figure 2-177

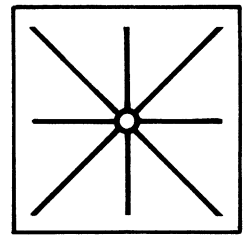


Figure 2-178

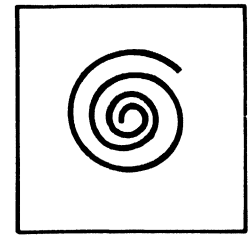


Figure 2-179

These improvements are not sufficient for large SCRs; thus different configurations were invented:

- field initiated gates
- amplifying gates

These SCR's were often complemented by use of fingers for the purpose of quickly triggering the maximum amount of silicon to avoid a localised rise in temperature. The result of these technologies is in the form of a small pilot thyristor which control the larger structure, thus resulting in less gate control for very good dI/dt (Figure 2-180).

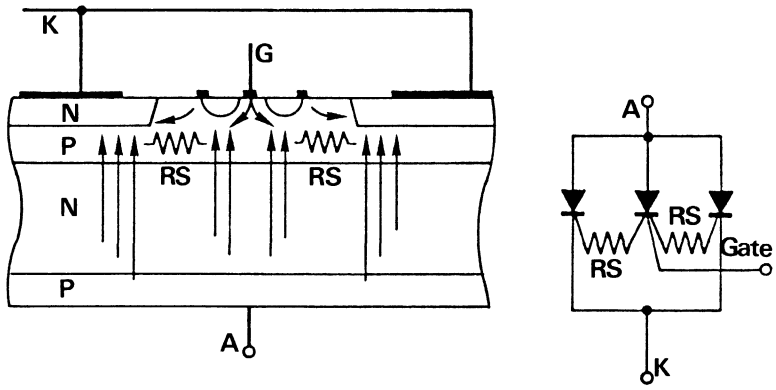


Figure 2-180 – Amplifying gate and symbolic representation of this type of structure

E-1.2.2. In what simple way can the dI/dt of 2 products be compared?

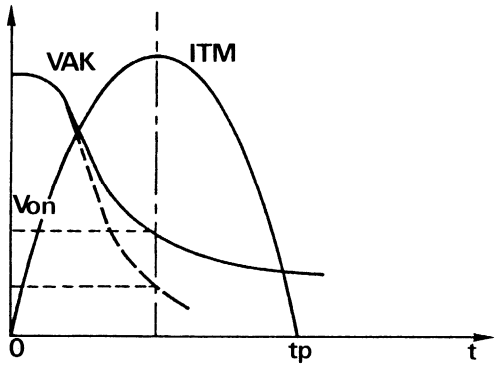


Figure 2-181 – dI/dt comparison

If a half sinewave of maximum current is conducting for a tp time of 10 to 20 microseconds, the voltage at the SCR terminals is as indicated in the Figure 2-181. The device with the maximum amount of die conducting at tp/2 is the one which has the highest dI/dt capability and also has the lowest Von.

E-1.2.3. For the user: slow down the rate of rise in current at the start of conduction.

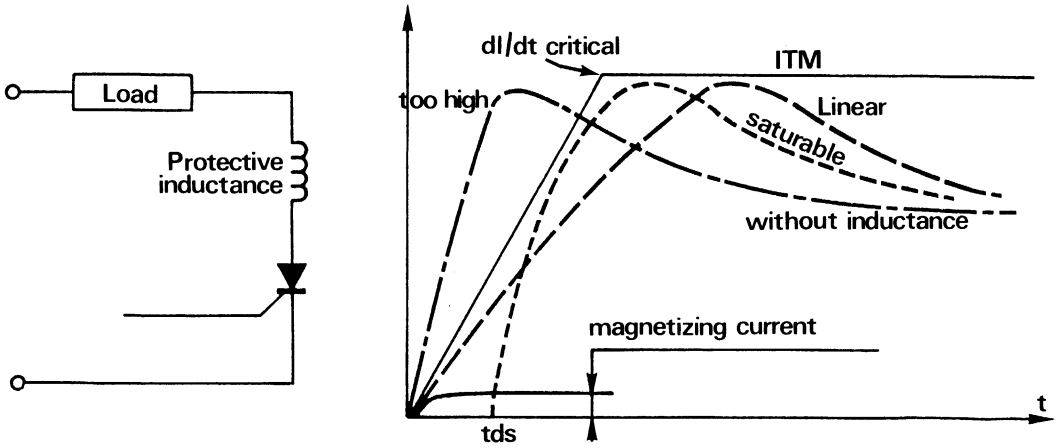


Figure 2-182 – Limitation of dI/dt

To begin with the pulsed gate current should have a fairly steep rise-time, with sufficient Igm/Igt ratio (see Figure 2-175), then, an inductance should by placed in series with the load and the SCR.

The question is what type of inductance: linear or saturable?

Figure 2-183, shows the effect at using the two different inductors on dI/dt.
It is shown from these turn off characteristics that the saturable inductor provides all the advantages: shorter turn off time and lower reverse voltage.

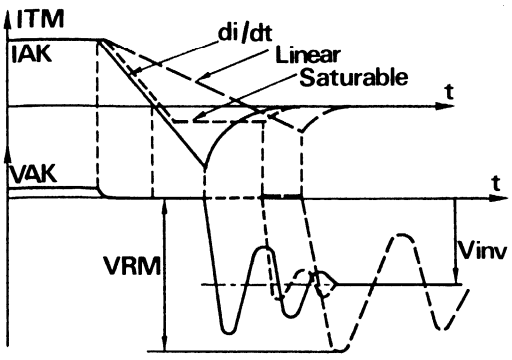


Figure 2-183 – Performance of different inductances at turn off

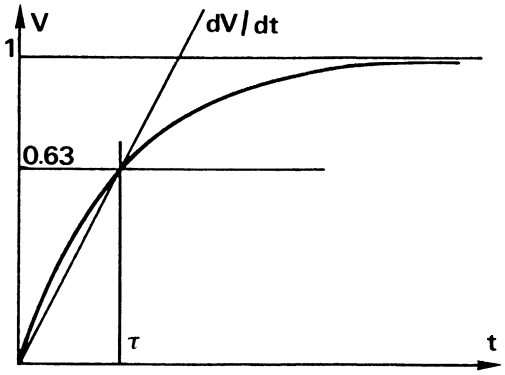


Figure 2-184 – Definition of dV/dt

The turn on delay time can be calculated by: $tds = \frac{n.A.\Delta B}{100 \times Vsupply}$ (microseconds)

n = number of turns, A = cm^2 of magnetic circuit area, ΔB = flux variation in Gauss. This with allow the maximum amount of silicon conducting when the main terminal current starts to flow. Amount of the magnetising current can also be calculated in order to obtain maximum silicon conduction Imagn: I X H_C, I = length of lines of force in cm, H_C: coercive force.

E-1.3. PROBLEMS OF dV/dt

When a fast rate of change of voltage dV/dt is applied to the anode of the SCR, a capacitive current, due to the reverse biased center junction capacitance, may be rejected into the gate of the SCR, as follows: Ic = C dV/dt. If sufficiently large, the SCR can be inadvertently turned on Figure 2-184, describes the definition of dV/dt.

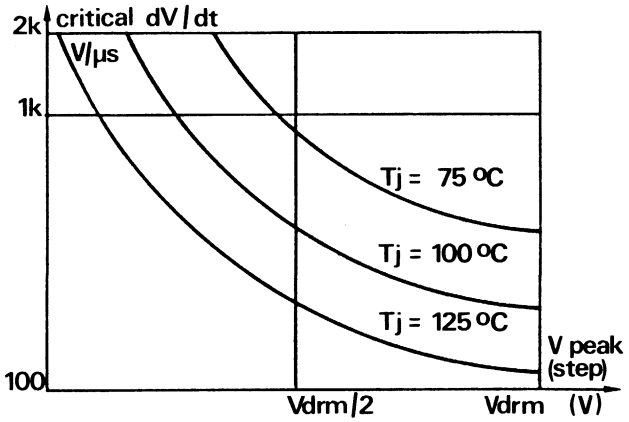
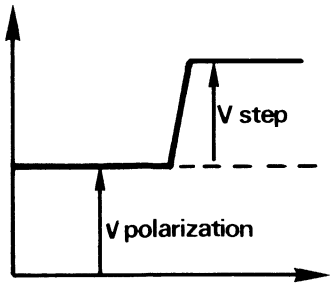


Figure 2-185 – dV/dt = f(Vpic)$|_{T°}$

This depends upon junction temperature and state of the device before application of dV/dt as shown in Figures 2-185 and 2-186.



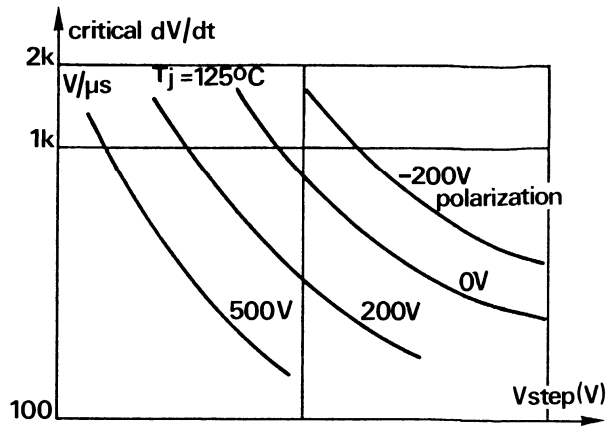


Figure 2-186 – dV/dt = f(Vstep) | polarisation

This dV/dt applied to the device when in a stable blocking state must not be confused with a different dV/dt parameter reapplied to the product when in unstable state just after turn off. This turn off condition will be described later.

How can dV/dt capability be improved?

E-3.1. FROM MANUFACTURERS STANDPOINT

The first solution for limiting the structures sensitivity to dV/dt is to place a resistance between gate and cathode allowing current i = C dV/dt to flow through a path other than gate – cathode injecting junction.

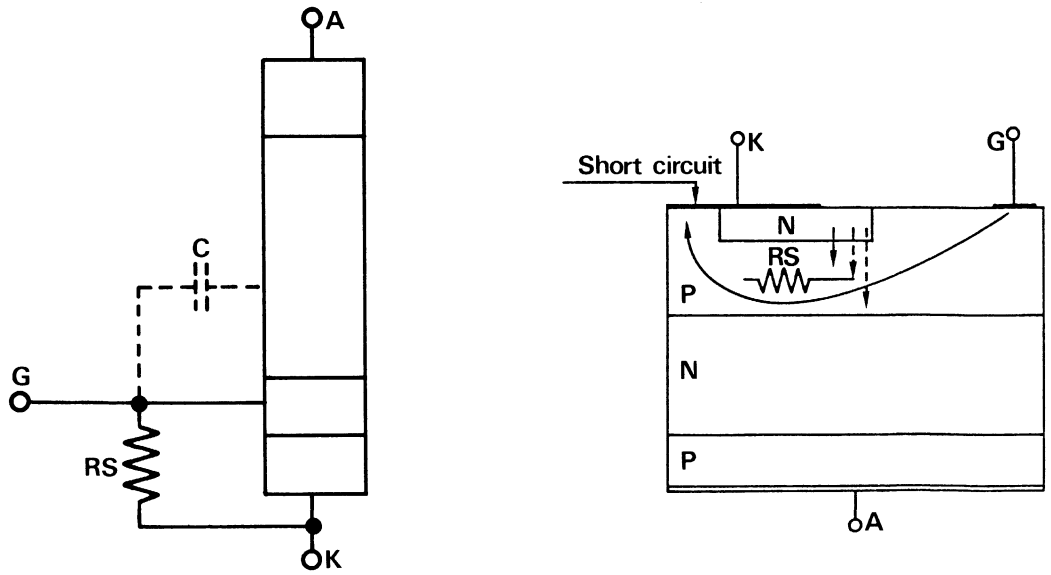


Figure 2-187 – Cathode in short circuit (shorted emitter)

One solution for resolving this problem is to use a certain length region of P resistance. Part of the cathode metalization overlays the cathode-gate junction producing a partial short circuit. By adjusting this metalization length, which is remote from the gate metalization, an internal gate-cathode resistor Rs is created. The resistor is designed so as to offer good dV/dt immunity and still not be too low to reduce drive efficiency.

This resistance also has the quality of improving SCR temperature characteristics by passing leakage currents.

E-3.2. FROM A USERS STANDPOINT

First the device must be chosen with high dV/dt capability in applications where untimely turn on would be dangerous.

Then, choose a device having VDRM, some what higher than the supply voltage, as shown in Figure 2-185. When Vpeak/VDRM decreases with increasing VDRM, sensitivity to dV/dt decreases.

Sensitivity to dV/dt can be reduced by negatively biasing the gate during the blocking mode: Figure 2-188.

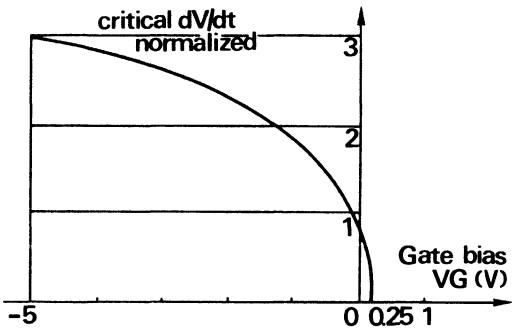


Figure 2-188 – dV/dt = f(Vg)

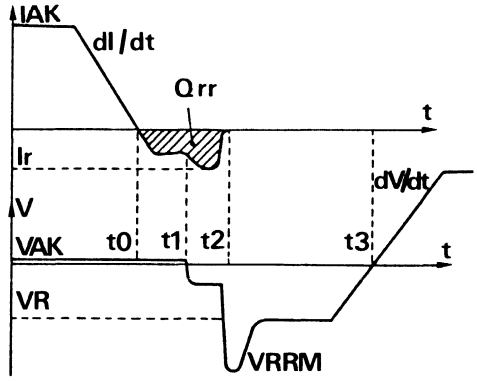


Figure 2-189 – SCR turn off

The use of snubbing networks will also reduce the dV/dt stress during turn off, as described in the following paragraph.

E-2. SCR turn off

To turn off an SCR (except a GTO), it is necessary that the load current pass below the holding current Ih.

Enough time must also be allowed for the carriers included in the structure to be dissapated (extraction and recombination) before reapplying the blocking voltage and this voltage can only be reapplied with dV/dt below a critical value.

When the load current passes through zero the minorities carriers that exist in the structure need to be expelled – resulting in a reverse current Ir.

VAK voltage remains positive and equal to about 0.7 V, the SCR operating at this moment as a current generator.

At time t1 the carriers around the gate-cathode junction are dissipated the junction becomes blocked and VAK begins to reverse.

Meanwhile the junction passes to avalanche state with VR being low due to high dopage. The current takes away the remaining carriers and the structure blocks at time t2.

Time t2 – t0 is called the **thyristor reverse recovery time trr** with Qrr being the recovered charge.

Meanwhile the minority carriers can still be found near the center junction: they can only disappear by recombination. This process is slow and direct voltage can only be reapplied within specified limits after a certain time t3; the interval of time t3 ± t0 is the **total thyristor turn off time tq**.

We shall now see which parameters influence Qrr, trr and tq.

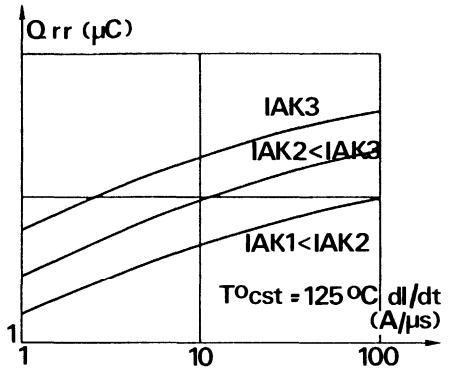


Figure 2-190 – Qrr = f(dI/dt)|IAK

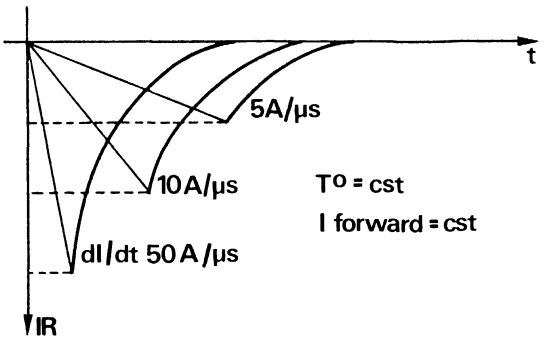


Figure 2-191 – Influence of dI/dt on Ir

We can see in this diagram that Ir approaches the forward current and Qrr increases for increasing dI/dt. On the other hand, for turn off time we have:

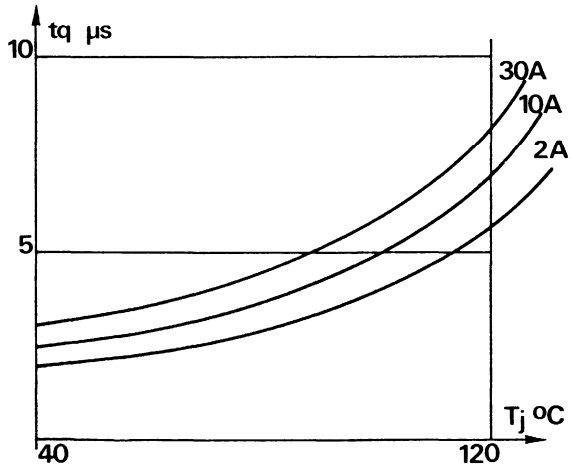


Figure 2-192 – tq = f(Tj)

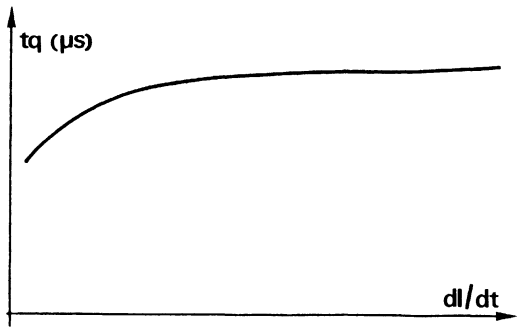


Figure 2-193 – tq = f(dI/dt)

tq increases more rapidly with junction temperature than with increasing anode current; the current influences tq only very slightly: Figures 2-192 and 2-193.

The turn off dI/dt also influences tq only very slightly but is on the contrary very influenced by reverse blocking voltage VR Figure 2-194.

It can be seen that tq varies by about 2 to 1 between 0 and 50 V after which it varies very little.

tq also increases by about 2 to 1 with increasing load. The magnitude of the reapplied dV/dt should be lower than the blocking voltage of the SCR as can be seen by Figure 2-195, tq increases somewhat with increasing dV/dt.

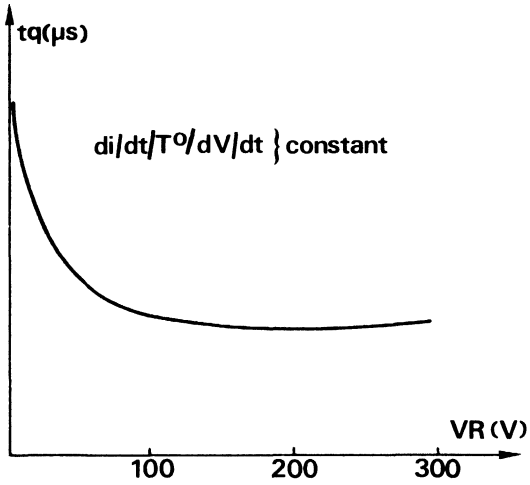


Figure 2-194 – tq = f(Vr)

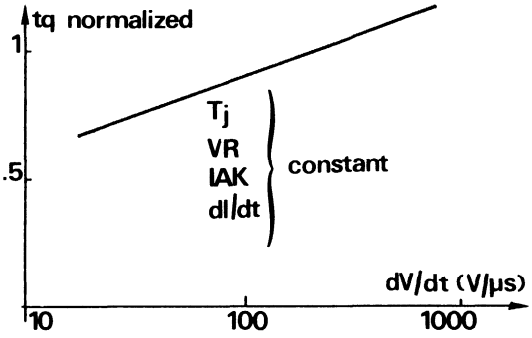


Figure 2-195 – tq = f(dV/dt)

dV/dt capability also varies with the dI/dt of the current during turn off: Figure 2-196.

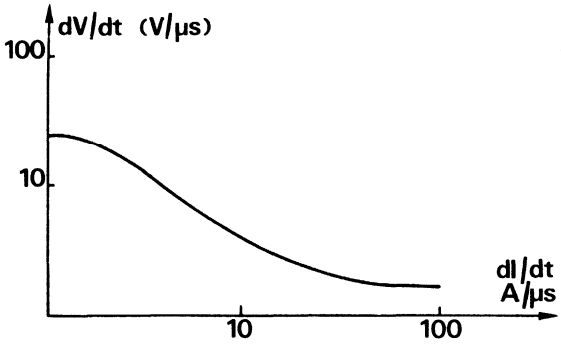


Figure 2-196 – dV/dt = f(dI/dt)

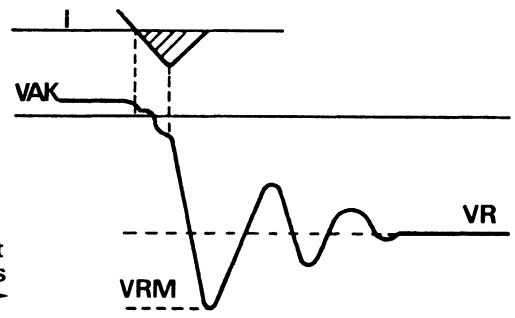


Figure 2-197 – Parasitic oscillations at turn off

For high dI/dt, junctions are quickly blocked and a strong dV/dt gradient cannot be reapplied.

What can be done to improve dV/dt capability? We have looked in the previous paragraphs on dV/dt characteristics at solutions suggested by manufacturers and the choices for users. For dynamic dV/dt, choices are identical but one can in addition use turn off aid circuits.

E-2.1. At the moment when the two SCR external junctions have dissipated their carriers, the structure blocks and reverse voltage oscillations may appear due to parasitic reactances in the network: Figure 2-197.

E-2.2. The same circuit can slow down the rise of the supply in a way that keeps it inside permitted limits: Figure 2-198.

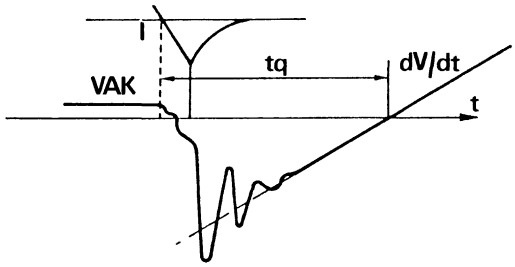


Figure 2-198 – dV/dt of rise of direct voltage

For this, there are several types of networks which can minimize dv/dt.

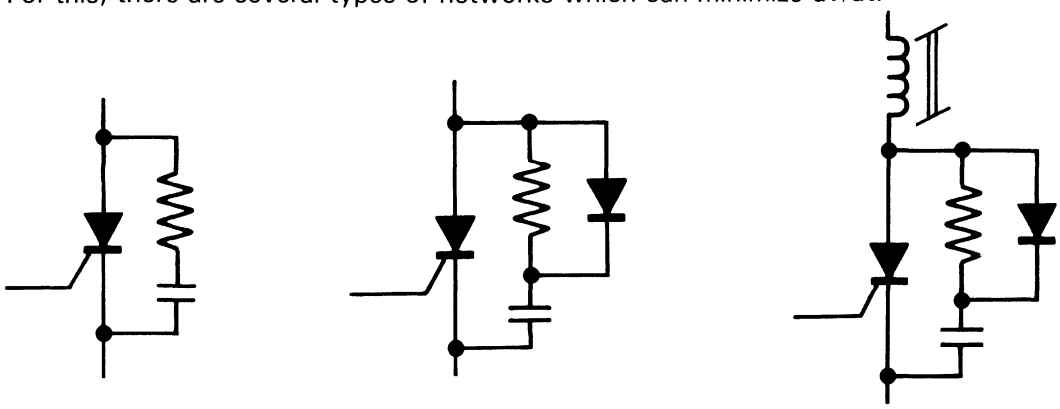


Figure 2-199 – Different switching aid circuits

The capacitor limits the abrupt rise of Vsupply and the resistance limits the capacitor discharge current when the SCR fires. The diode allows the use at the maximum capacitance at turn off without stressing the SCR on firing. Values of R and C can be approximately calculated for a given SCR, and then adjusted for the desired results, bearing in mind that C must be as small as possible as losses in this circuit = $1/2\ CV^2$.

As an example: C = Qrr/V at the start of cut off.

This shows the advantage of having Qrr as small as possible. (Figure 2-190). For an SCR with Qrr = 100 μC, for example, and power voltage supply of VAL = 500 V, C = $10^{-5}/500 = 0.2\ \mu$F. R is designed to keep the maximum current on firing below ITM. If ITM is 20 A: R = 500 V/20 A = 25 Ω.

Therefore: RC = 5 μs and dV/dt = 0.63 VAL/RC = 300/5 = 60 V/μs which is highly acceptable. Energy dissipated is
$1/2\ CV^2 = 1/2\ 0.2 \times 10^{-6} \times 25\ 10^4 = 0.025$ Joules.

Power dissipated is 25 W for a frequency of 1 KHz, which should be dissipated in the resistor R. The overvoltage at turn off is approximately: $\Delta V = Ih/\sqrt{L/C}$.

It is estimated that the parasitic wiring inductance is about 1 nH/mm of wire. For the case of 3.2 μH of parasitic inductance, $\Delta V = 20\sqrt{3.2/0.2} = 80$ V. which is 16% of the power supply.

E-3. SCR overload characteristics

E-3.1. SCRs are specified for current ranges, both repetitive and not repetitive, which guarantees that the junction temperature will be below the maximum specified temperature.

Example: MCR 221: Tj max = 125°C, $R\theta jc$ TO 220 = 1.5°C/W. IRMS = 16 A for TC = 90°C, for IRMS = 16 A, Imax = $16\sqrt{2}$ = 22.7 A pk, for Imax = 22.7 A, VT = 1.5 V pk typical VT = 1.5 V resulting in the power dissipated Pd = Imax VT/4 = 22.7 × 1.5/4 = 8.5 Watts and Tj-c = $R\theta jc$ × PD = 8.5 × 1.5 = 13°C. Therefore, Tj = Tj-c + Tc = 90 + 13 = 103°C < 125°C.

E-3.2. SCRs are also rated for surge current conditions on a non-repetitive basis. These overload surges are limited, however, to one hundred occurrences over the life of the device.

An overload can only be applied when the junction temperature is below the junction temperature limit.

It is also clear that SCR blocking parameters can only be guaranteed if the temperature reverts to its specified value particularly for turn off time tq, reapplied dV/dt etc.

The number of sinusoïdal cycles of 60 Kz is generally given, also the maximum current for each of these cycles. The circuit fusing specification I^2t is also shown for 1/2 cycle, sinusoided pulses of 1ms to 8.3 ms (60 Hz).

E-3.3. Peak non-repetitive forward surge current

This surge current specification is based on a 1/2 cycle sine wave of 60 Hz (8.3 ms). It may be applied once junction temperature is at its maximum.

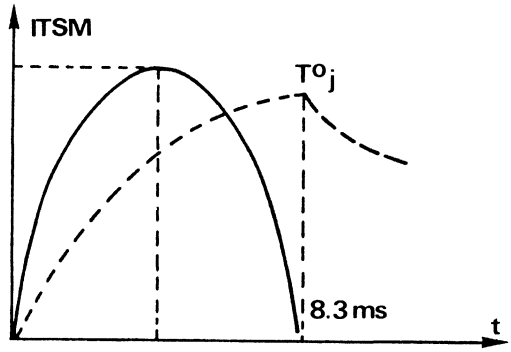


Figure 2-200 – Single overload (surge: ITSM)

Several half sinusoid pulses may be allowed according to the following curve: MCR 221: Figure 2-201.

As an example, for 5 8.3 ms cycles (total time of 83 ms), the maximum current for each cycle cannot exceed 125 A.

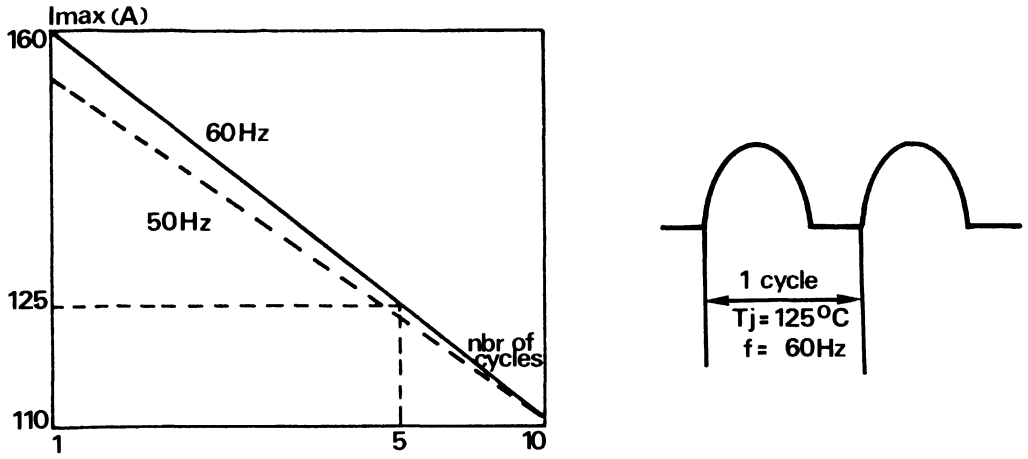


Figure 2-201 – Overload for several cycles

E-3.4. I^2t

An even higher Imax for cycles less than 8.3 ms can be calculated since heat transfer is linear and thus proportional to $\sqrt{t}$, $I^2\sqrt{t}$ = Energy = constant, i.e. for 1/4 the initial time, I^2 becomes twice the initial I^2 and thus 1.41 times the initial current.

Example: MCR 221.

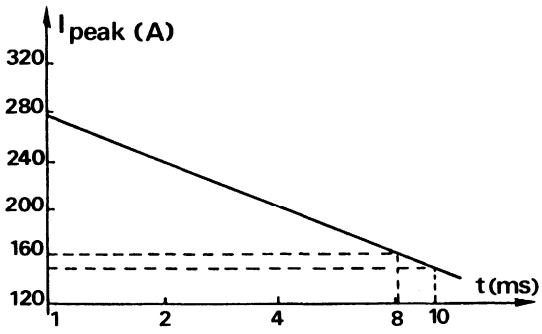


Figure 2-202 – Ipeak = f(t)

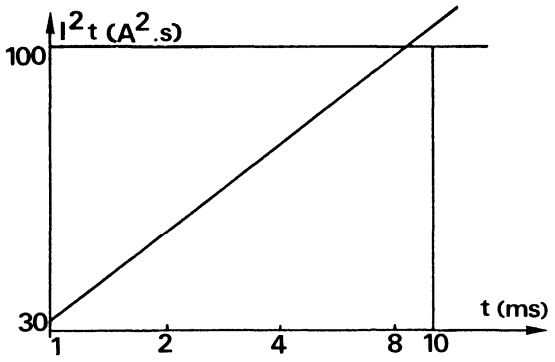


Figure 2-203 – I^2t = f(t)

From the curve for t = 8.3 ms, Ipeak = 160 A, and for 10 ms, Ipeak = 152 A.

Extrapolation of this data results in the dotted curve in Figure 2-201, (50 Hz). Also, point by point calculation of I^2f results in the curve of Figure 2-203, noting that I in I^2t is an RMS value (root-mean square).

As an example: I^2t for 8.3 ms = $(\frac{160}{\sqrt{2}})^2 \times 8{,}3\ 10^{-3} \cong 100\ A^2.s$ and for t = 1 ms

Ipeak = 270 A, $I^2t = (\frac{270}{\sqrt{2}})^2\ 10^{-3} = 36\ A^2.s$

F) Series connection of SCRs

Although SCRs as high as 5 kV are on the market, it is sometimes more economical to connect the SCRs in series for special high voltage application.

If several SCRs of the same type are mounted in series, the normal distribution of static and dynamic parameters do not always guarantee a practical design.

F-1. Let us take first the case of blocking voltage

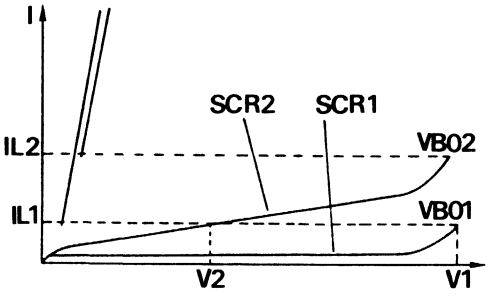


Figure 2-204 – Distribution of static characteristics of two SCRs

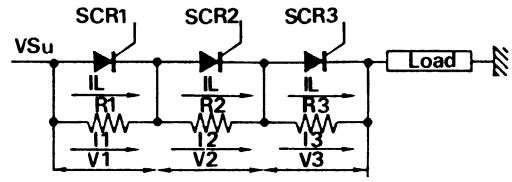


Figure 2-205 – Series equalisation network

Instead of having a blocking voltage of $2V_1$ as required, due to leakage current IL_2, $V_1 + V_2 < 2V_1$. The solution to these mismatched parameters is to bridge the SCRs with the illustrated resistor network (Figure 2-204) to equal potentials across each SCR.

The worst case arises when one device has minimum leakage current IL and the other, a maximum current: the voltage division would be inverse proportional to the leakage current.

If R1 = R2 = R3 = R and SCR1 supports the maximum voltage, V1 = RI1 and Vsupply = V1 + (n – 1) RI2,(If $I_2 = I_3$) and SCR2 IL = SCR3 IL, I1–I2 = ΔIL maximum currents distribution of a given type SCRs.

Therefore VAL = V1 + (n – 1) R (I1 – ΔIL), or, VAL = V1 + nRI1 – RI1 – nΔILR + ΔILR, or, VAL = nRI1 + (1 – n) RΔIL and R = (VAL – nV1)/(1-n) ΔI_L.

If V1, is the maximum voltage of this SCR series which is equal to V_{DRM}, the worst case is when IL min = 0.

Therefore ΔIL = IL = IDRM and R = (n.VDRM – Vsupply)/(n-1) IDRM. The resistance R should be as large as possible to minimize losses P = V^2/R.

It is important to select SCRs with low ΔI_{LS} at the maximum operating temperature, as the equation for calculating the resistor indicates.

F-2. Dynamic balancing of series SCRs

During switching (dynamic), the slowest SCR could have to support the full supply voltage unless a voltage equalization network, using parallel capacitors, were used (Figure 2-206). To minimize voltage unbalance the capacitor should be as large as possible

since dV/dt = I/C. However, these large capacitors charged during turn off will be discharged during turn on producing possibly large and harmful surge currents to the SCR.
This current should thus be limited by a series capacitance as shows by the classic switching aid network (snubbing network) of Figure 2-206.

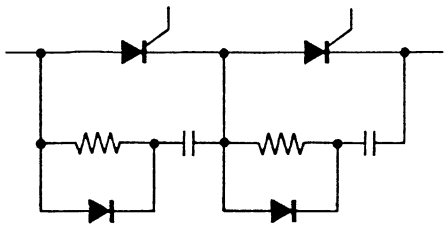


Figure 2-206 – Switching aid network

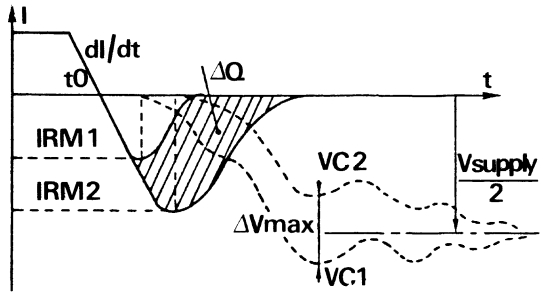


Figure 2-207 – Recovered currents and voltage at capacitance terminals at cut off

At cut off, this equalisation network will be extremely useful for allowing the passage of current of the slowest device through the area of faster devices.
Let us take the unfavourable case of SCR having maximum dispersion of recovered load Qrr: Figure 2-207.

Due to the difference in recovered charge in the 2 SCR, the capacitance shunts do not load equaly and a potential difference may result $\Delta V_{max} = \Delta Q_{max}/C$.
This difference will decay with time according to formula $\Delta V = \Delta V_{max} \exp(-t/RC)$ where $\Delta V_{max} = nV_{DRM} - V_{supply}$ with n being the number of devices.
For the worst case, a device that is much slower than the others, the difference of recovery charge is $\Delta Q = (n-1)\,\Delta Q_{max}$.

Resulting in $$C = \frac{(n-1)\quad \Delta Q\ max}{VDRM - Vsupply}$$

Since Qrr depends on operating conditions it is not possible to reduce to maximum C to reduce losses = $1/2\ CV^2$.
Qmax can be reduced by lowering dI/dt, Imax and temperature. The resistance R in series for turn on can be determined by:

$$R = \frac{VSCR}{Ipeak\ maxim} = \frac{VSCR}{ITSM}$$

This resistance also has a damping effect on the loop: RC, parasitic inductances due to the circuit.

α = R/2 $\sqrt{C/L}$. With overvoltage of Vpeak = I $\sqrt{L/C}$.

Thus, for a good damping factor (large α) and minimum overvoltage, C should be as large as possible. A compromise must be made between C minimum for minimum losses and C maximum for good damping factor. Clearly this compromise can be simplified by making the parasitic L as low as possible by making the interconnection leads as short as possible. For minimum C, α should be between 0,5 and 1.

Also the R – C time constant should be well below the conduction period RC $\leq$ tp/5 in order to allow complete charging and discharging of the capacitor. The rate of voltage rise should also be kept below minimum dV/dt of reapplied voltage dV/dt = 0.63, Vsupply/RC. Finally, R must be able to dissipate 1/2 CV^2f.

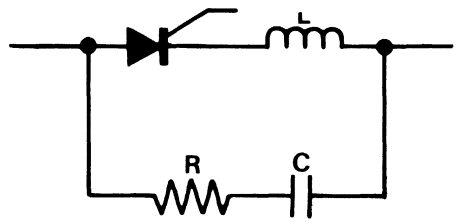


Figure 2-208 – Dynamic balancing network

G) Paralleling of SCRs

Some of the large SCRs available today can carry currents greater than 2 kA, paralleling is not often used.

However if one wishes to parallel these products because of manufacturing, costs these is a risk, as with all parallel devices of large variations in current sharing.

Solutions are the same for all semiconductors: bipolar transistors, power MOSfets, etc...

Select products with static and dynamic characteristics at operating temperatures:

- use control networks which reduce switching time
- good layout to minimize deviation of ballast and control network characteristics
- symmetric thermal layout between devices
- use external ballast networks: series resistance: but very dissipatory, dynamic ballasting transformer: very expensive.

H) The Triac

The triac, which is a bidirectional switch with 3 electrodes (Triode AC semiconductor), switches on in exactly the same way as the SCR.

Its function is identical to that of 2 SCR connected in an anti-parallel configuration.

The triac as several limitations (dV/dt, dI/dt) which presently allow devices with 50 A and 800 V capabilities, for greater power requirements, two anti-parallel connected SCRs are generally useds.

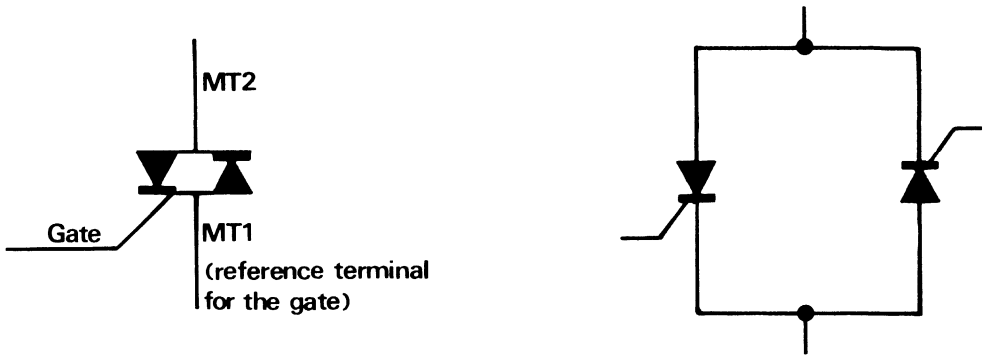


Figure 2-209 – Triac symbol and equivalent anti-parallel SCR configuration

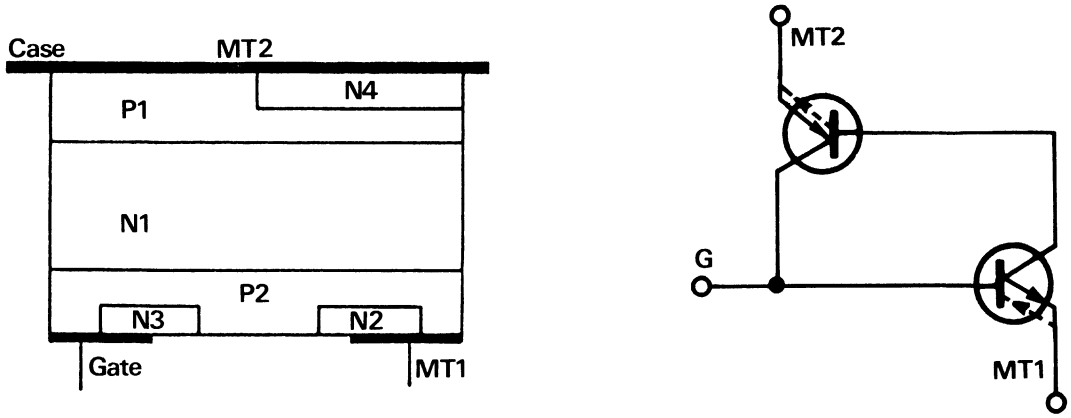


Figure 2-210 – Technological representation of triac

The left half the triac structure consists of an SCR P1 N1 P2 N2 and gate P2 N2 and on the right of the structure, the opposite SCR N4 P1 N1 P2 and gate N3 P2.

H-1. Static characteristics of triac

Figure 2-211 describes the symmetrical characteristics of the 2 anti-parallel SCRs. For the gate control characteristic, there are 4 possibilities.

- positive gate control VG – MT1 > 0
- positive voltage supply → quadrant I
- negative voltage supply → quadrant IV
- negative gate control VG – MT1 < 0
- positive voltage supply quadrant II
- negative voltage supply quadrant III

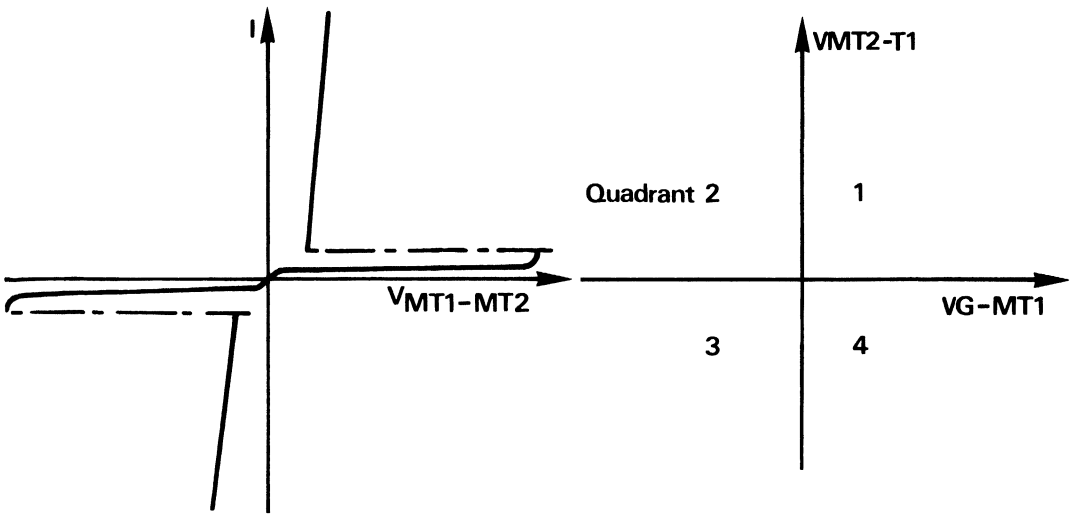


Figure 2-211 – I = f(V) and V = f(VG)

H-2. Working diagrams for four quadrants

H-2.1. VG > 0, MT2 > MT1 = classic thyristor working.

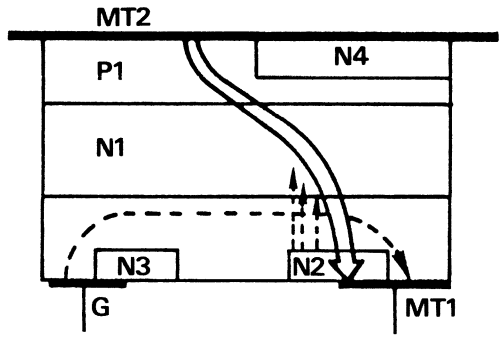


Figure 2-212 – Quadrant I

Metallization of MT1 creates a short circuit N2 P2 (shorted emitter). This lateral resistance increases dV/dt capability.

H-2.2. VG < 0, MT2 > MT1 = quadrant II
The main structure is still P1 P2 N2, gate P2 N3

The small diagram shows the equivalent NPN transistor (N1 P2 N3). If current is removed through the gate (VG < 0) this transistor is fired. Structure MT2 – MT1 remains on, even if the control voltage is removed from N3.

The rise in energy of junction N3 (G–) allows firing of the structure: the electrons can get through the first barrier and thus create thyristor type firing of the auxiliary structure, thus allowing, in turn, firing of the main structure.

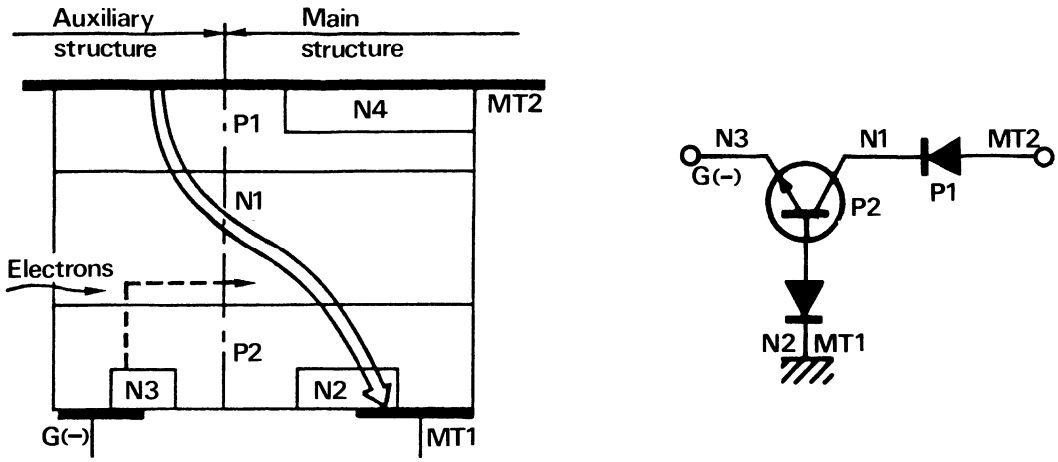


Figure 2-213 – Quadrant II

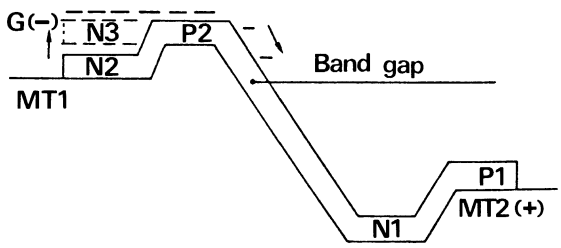


Figure 2-214 – Diagram of firing in quadrant II

H-2.3. VG < 0, MT1 > MT2: quadrant III. Now the main structure is inverted P2 N1 P1 N4 and gate is N3 P2.

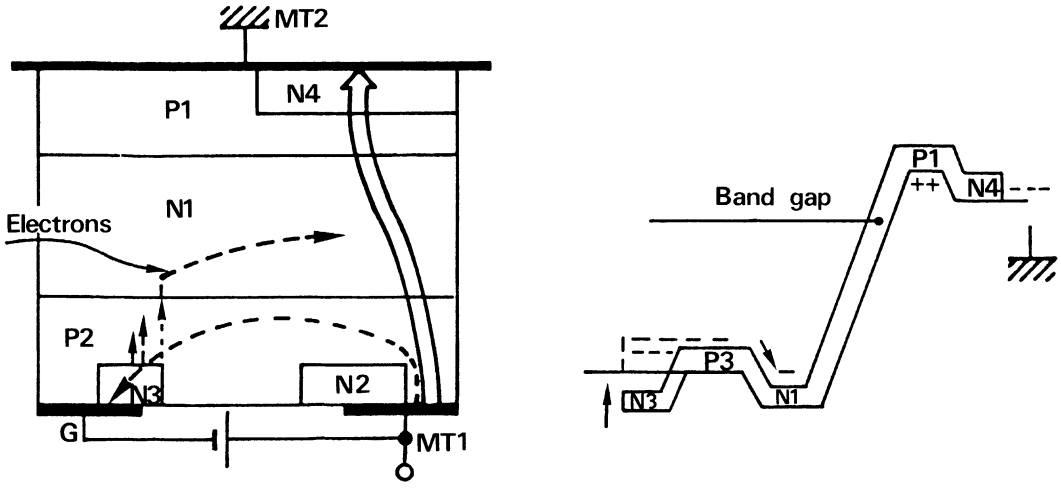


Figure 2-215 – Firing technique in quadrant III

This firing is called "remote – gate" as triggering is now accomplished through one of the internal bases of the composite transistors (P2 for transistor NPN and N1 for transistor PNP).

On the diagram showing the Band gap the negative bias of the gate raises the energy from zone N3 enabling electrons to get through the first barrier N3 P2; then the electrons fill the N1 space increasing its energy. Holes taken into P2 can now go back up into depletion zone N1 (less energy for the holes) then, lowering P1 energy and allowing electrons and holes to circulate.

H-2.4. VG > 0, MT1 > MT2 – Quadrant IV

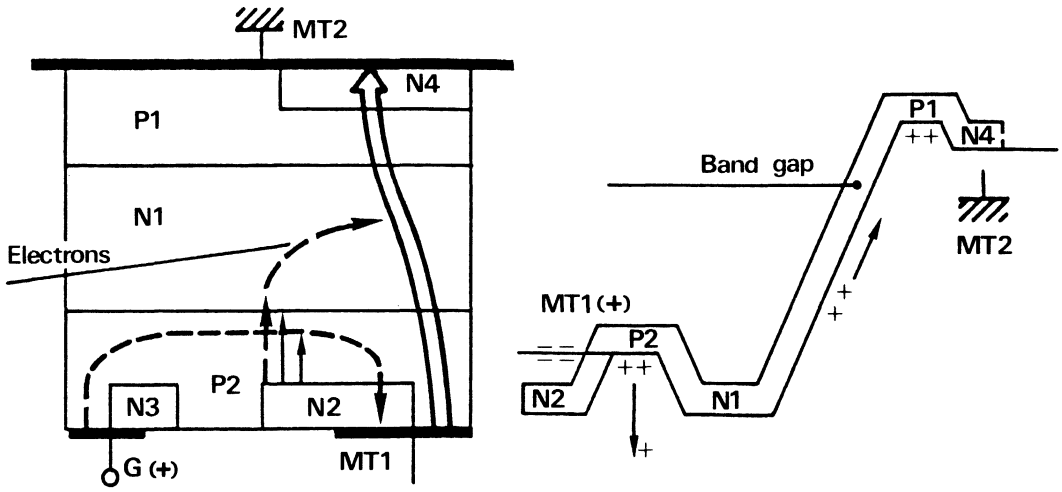


Figure 2-216 – Firing in quadrant IV

The main structure is P2 N1 P1 N4 and gate P2 N2.

Junction P2 N2 is forward biased and injects electrons collected by N1. Holes can move across N1 depletion zone and accumulate in P1 finally to be collected by N4, causing the device to fire.

H-3. Dynamic characteristics of Triac

As general rule, rules for SCRs can be directly applied to triacs. The triac, because of their 4 quadrants of control, have certain special performance which shall be looked at.

The best switching performance occurs in quadrant I (normal thyristor), the worst is in quadrant IV: this is why many triacs are not specified for this quadrant and it is better, anyway, for reliability purposes, not to use it. Quadrants II and III are far more uniform current flowing immediately when triac control is switched on, preferably by negative logic. As the triac is a device containing 2 internal SCRs, conduction of one of the 2 SCRs affects the performance of the other. Because of this, the susceptibility to dV/dt is greater than for an SCR, being about 5 to 10 V/μs (compared to as high as 1000 V/μs for the SCR).

This dV/dt may be improved by having dead time between the end of the conduction cycle and the start of the next.

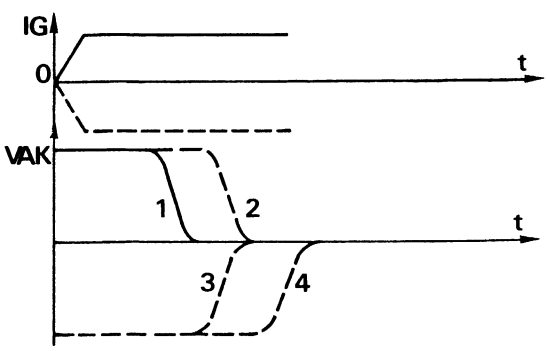


Figure 2-217 – Triac conduction performance in the 4 quadrants

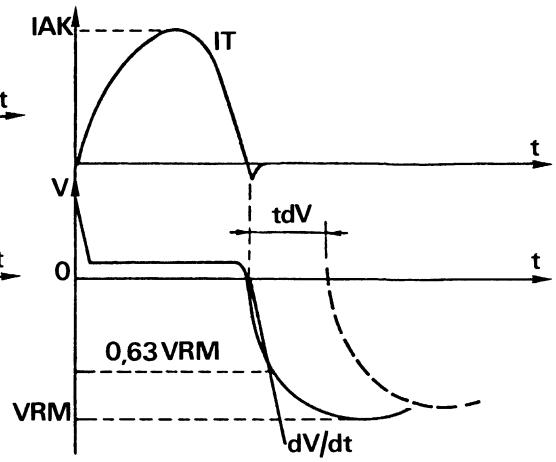


Figure 2-218 – dV/dt directly reapplied or delayed by tdV

This dV/dt is also very dependant on the junction temperature and the rate of charge of current – dI/dt.

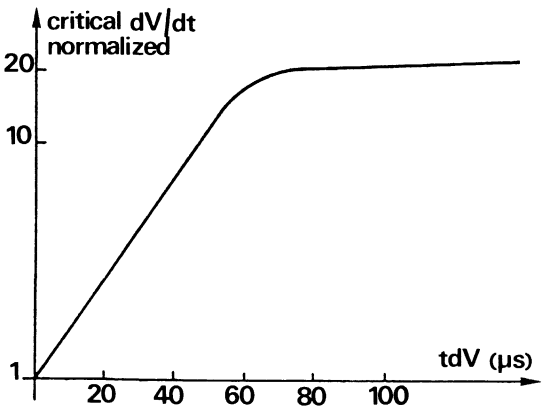


Figure 2-219 – Possible increase of dV/dt by increase of tdV dead time

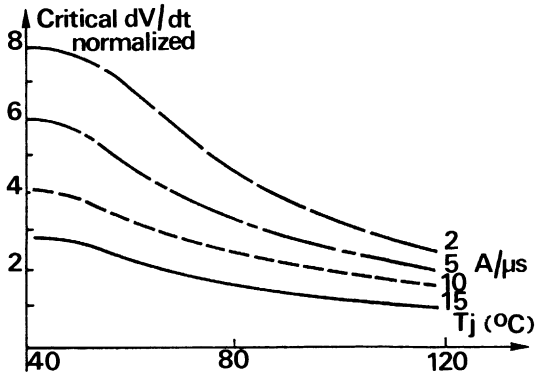


Figure 2-220 – dV/dt = f(Tj) | dI/dt

I) Triac control by existing logic

Such triacs as the BT158 (8-12A) and BT162 (15A) are characterized for quadrants I-II-III control where as the MAC15A has all four quadrants specified. These triacs have an Igt (max) of 75 mA, thus requiring at least 80 to 100 mA control. A simple way of interfacing TTL with the triac is use the PNP TO-92 small signal transistor BC327 which has an HFE of 100 at 100 mA.

MOS logics have 10 mA per gate but as there are four gates in each case, 40 mA can be obtained by putting them in parallel.

MECL can sink 50 mA but swing of outgoing voltage is only 800mV pk to pk to interface with the triac, by thus requiring the same TO92.

I-1. Control by TTL

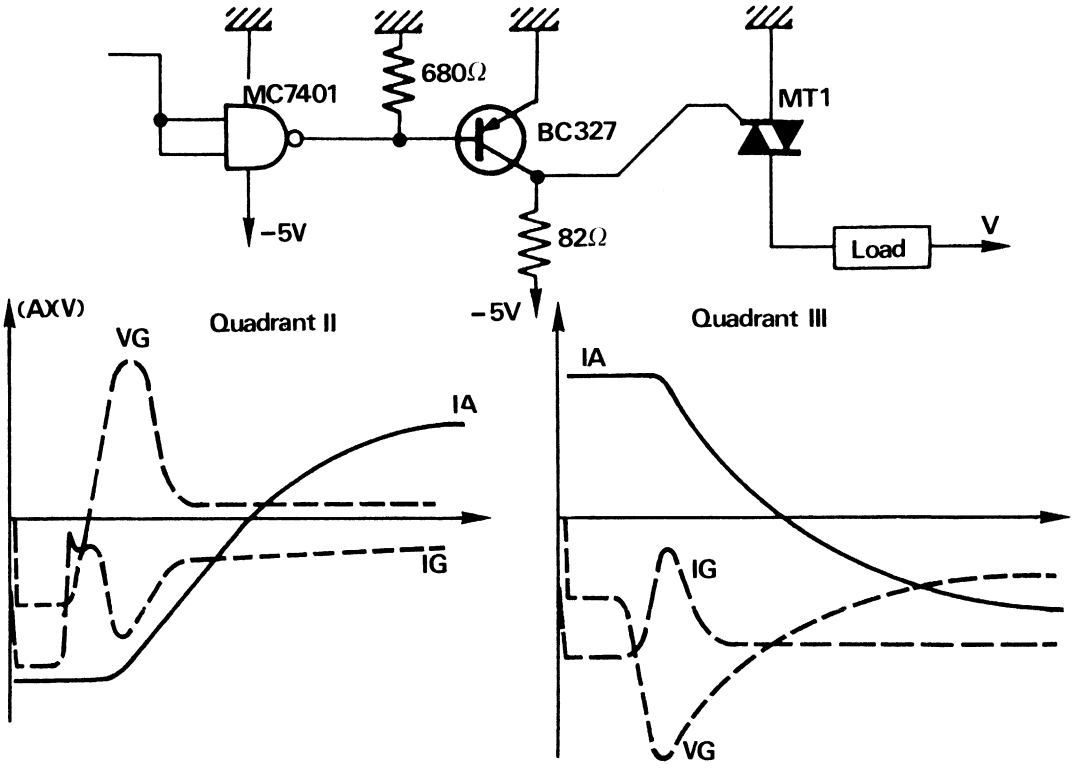


Figure 2-221

Table 2-15

IA	TRIAC		Quadrant II VG	IG mA	td µs	tr µs	Quadrant III VG	IG mA	td µs	tr µs
8	BT158		1	80	2	8	0.7	85	3	10
12	BT162		1.1	85	2	10	1	50	3.5	11
15	MAC15A	II III	0.8	50	2	8	0.8	50	3.5	10
		I IV	1	50	1	8	1	50	4	10

With this form of control, switching times obtained are very consistent. Delay time: 2 microseconds. Rise time on resistive load: approximately 10 microseconds.

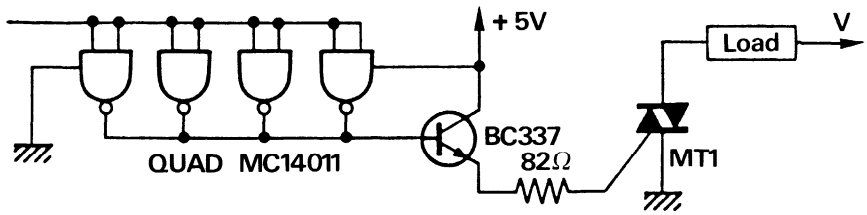


Figure 2-221 – Control by TTL

I-2. Control by MOS logic

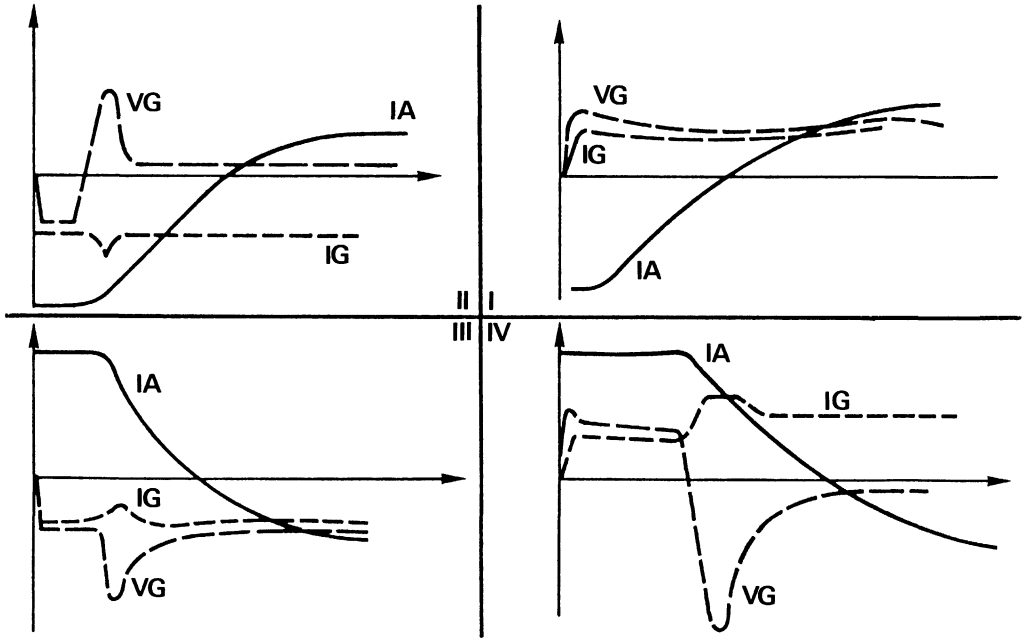


Figure 2-222

Table 2-16

		VG	IG	td	tr	VG	IG	td	tr
MAC15A	I IV	1.5	40	1	8	1.5	40	5	10
	II III	0.8	50	2	8	1	50	3.5	9

More uniform control is formed in quadrants II and III, good in quadrant I and fair but still acceptable in quadrant IV:

td of 2 to 5 microseconds
tr of 8 to 10 microseconds

I-3. Control by MECL logic

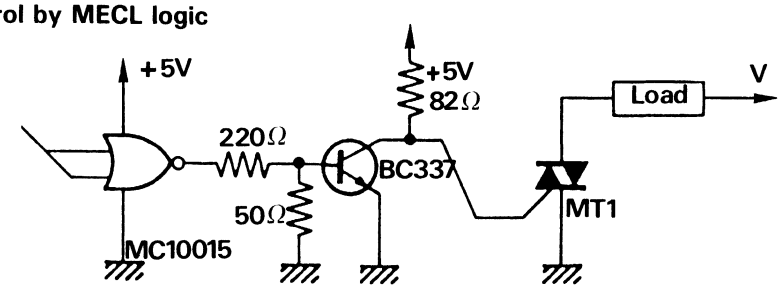


Figure 2-222 – Control by C MOS

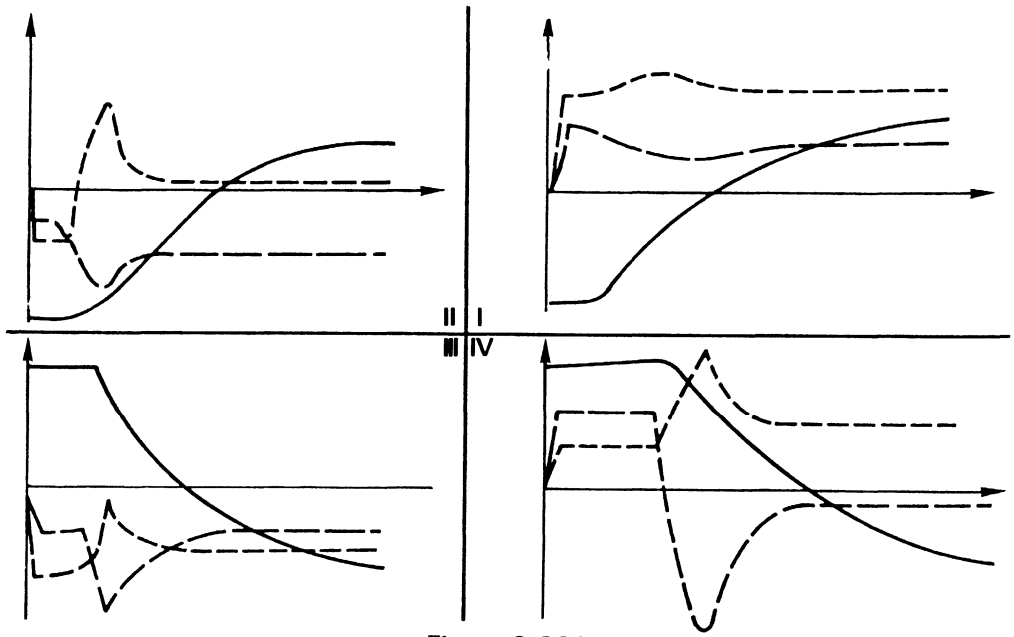


Figure 2-223

Table 2-17

		VG	IG	td	tr	VG	IG	td	tr
MAC15A	I IV	1.5	50	1	8	1.5	70	4	9
	II III	0.8	50	2	8	0.8	80	3.5	9

I-4. Conclusion

Combining all controls, shows that the variations in switching times obtained are very low, for delay time td.

Table 2-18

Quadrants μs	I	II	III	IV
TTL	1	2	3.5	4
C MOS	1	2	3.5	5
MECL	1	2	3.5	4

And for current rise time on resistive load: tr.

Table 2-19

Quadrants μs	I	II	III	IV
TTL	8	8	10	10
C MOS	8	8	9	10
MECL	8	8	9	9

J) The GTO thyristor

J-1. Plan of GTO

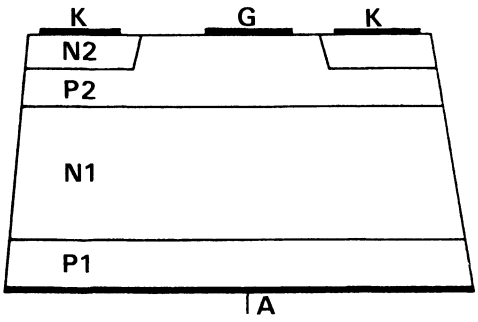


Figure 2-224 – Cross section of GTO

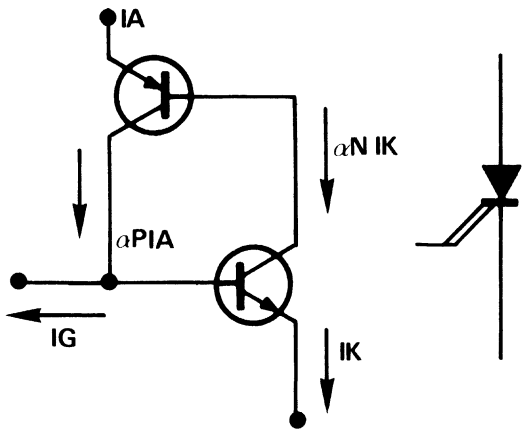


Figure 2-225 – Symbolic diagram of the 2 transistors

A GTO is an SCR where the turn off control is produced by removing current from the gate (base P of NPN transistor shown Figure 2-225) thus reducing the composite transistors gain.

J-2. Operation and turning off the device

SCR passive state can be written as: $IA = \alpha PF\ IA + \alpha NF\ IK$, αPF and αNF are the forced gains of transistor in saturation as $IA = I$ therefore $\alpha PF + \alpha NF = 1$.

To turn off the device, it is necessary that the extracted base current be higher than internal currents.

Giving $IG > \alpha PF\ IA + \alpha N\ IK - IK$.

At the limit, a minimum of current equal to SCR operating gain must be extracted with $IA = \alpha P\ IA + \alpha N\ (IA + IG)$ because $IK = IA + IG$, giving

$$IGmin = \boxed{\frac{\alpha N + \alpha P - 1}{\alpha N}\ IA}$$ and the control gain at turn on

$$\boxed{Gmax = \frac{IA}{IGmin} = \frac{\alpha N}{\alpha N + \alpha P - 1}}$$ the maximum gain limit with αN and αP transistor gains for IA current. At low current levels $\alpha N + \alpha P$ is very different from 1 and G can become very large, there is even a current (maintaining current) which naturally gives $\alpha N + \alpha P = 1$ and the device turn off by itself.

In a classic device, the current gain of the NPN transistor is made as large as possible (≈ 1), resulting in: $\boxed{Glimit = 1/\alpha P}$

This shows, the importance of the PNP transistor in a GTO.

As αP is proportional to the τ : carrier lifetime, it becomes very important to obtain maximum gain.

However, the total theory of this device is not completly developed at this time as many phenomena must be taken into account and the gain limit of the devices commercially available are around 15 to 20, much power than expected by the present homely theories.

In any case, it is currently accepted that G limit cannot be increased without paying the price of a higher holding current, thus difficult firing and higher saturation voltage.

J-3. Performance at turn off

For normal operation, the current density is more or less distributed through the volume of the component.

At turn off, removed of carriers through the gate causes a lateral field which increases the density of the charge current in the area furthest from the gate (load current staying constant during storage time ts). This high density of current is harmful at turn off because of localized heating. There is another harmful phenomenon: the appearance of a voltage between cathode gate at turn off, sufficiently large as to reach breakdown of the P2 N2 junction. If this junction breakdown the GTO can no longer turn off and the current removed at the gate is avalanche current. This explains the present maximum limit of load currents which can be turned off by the GTO.

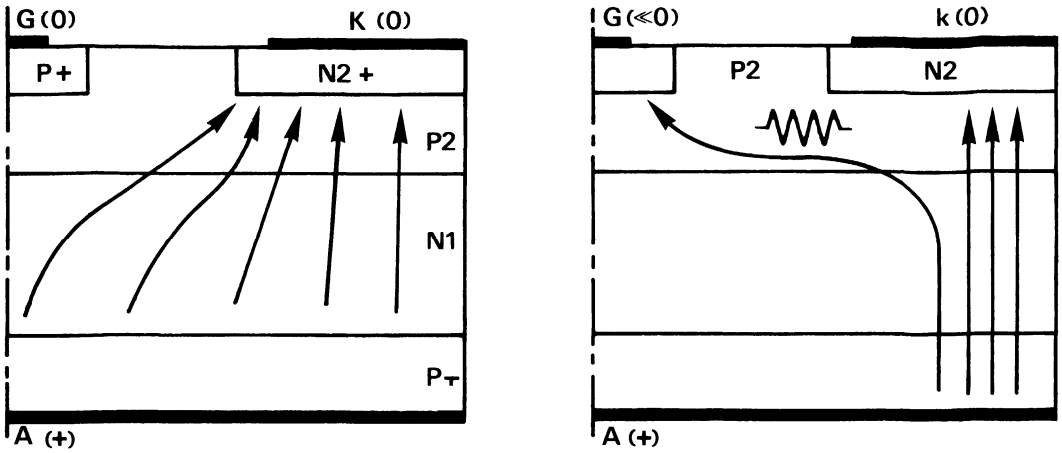


Figure 2-226 – Current distributor at turn off of a GTO

J-4. Technological solutions for the GTO

J-4.1. One of the solution for improving GTO turn off is to lower the resistivity of P layer crossed by gate current, but to keep a P zone sufficiently resistive in contact with the cathode to yield breakdown voltages sufficiently high.

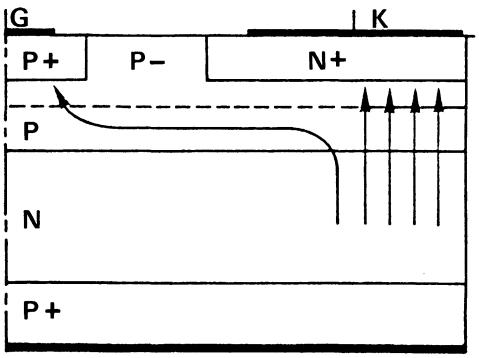


Figure 2-227 – Improvement of PN + junction

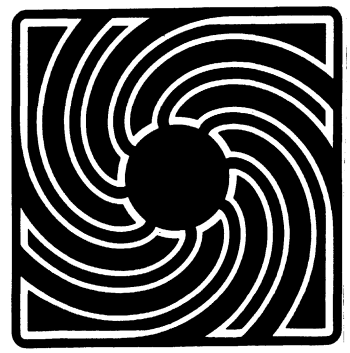


Figure 2-228 – GTO Motorola gate

Another, more sophisticated solution is to improve the lateral voltage drop due to IG and increase the surface of the current crowding zone, thus diminishing the density of current. This is accomplishead by an interdigited or ramified cathode structure.

J-4.2. The technology of "shorted emitters", which desensitizes the device to false turn on, is not suitable for GTOs since high, gate-cathode sensivity is required. But thanks to the highly ramified structures chosen for these devices and to the reduction of operating lifetime of the carriers in order to have good gain at turn on, devices exist with good dV/dt (500 – 1000 V/μs).

J-4.3. To reduce αP and thus the carrier lifetime the N zone can be doped with gold, although the temperature characteristics are not as good.

J-4.4. Another solution to improve blocking voltage at turn on is to create an anode short circuit. This is the way an asymmetrical GTO is obtained (anode shorted to emitter)...

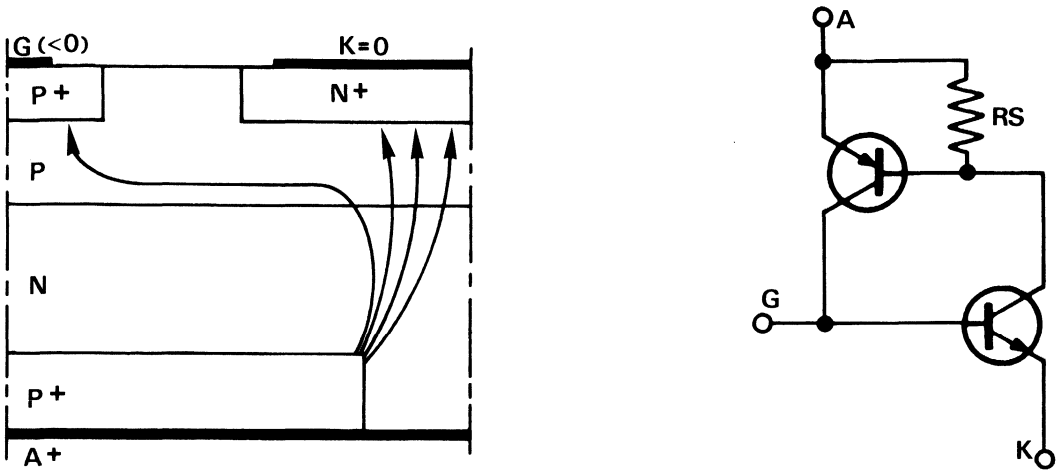


Figure 2-229 – Anode shorted to emitter

When current lines concentrated in the external section, only one N+PN non-regenerative structure remains which forces the plasma to extinguish itself. Obviously the reverse blocking of the GTO is limited to that of the PN+ junction, i.e. about 10 volts. To avoid this situation, a series or antiparallel diode can be added.

J-5. Static characteristics of GTO

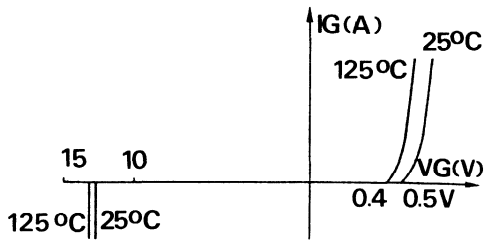


Figure 2-230 – Control characteristic IG = f(VG)

The forward characteristic is a diode and the reverse characteristics of a zener (10-15 V).

The SCR characteristic at the GTO is classic except when the IG critical at turn on is less than IG; in this case, the device behaves like a high voltage transistor. The gain of this transistor can be shown as follows: Figure 2-232.

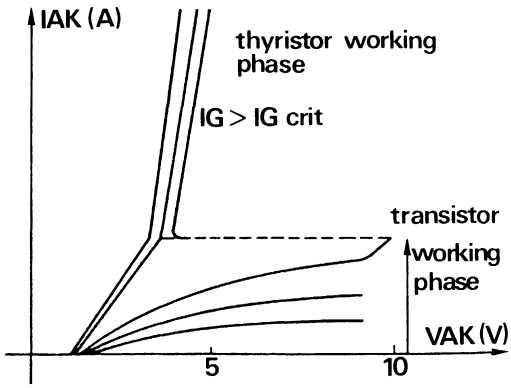


Figure 2-231 – Static characteristic of GTO IAK = f(VAK)

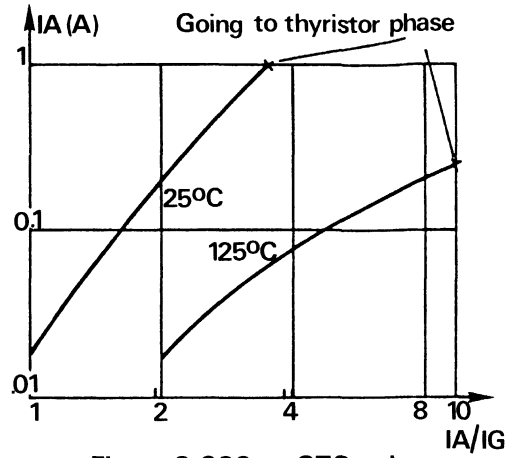


Figure 2-232 – GTO gain below critical IG

J-6. Turn on

The critical control current is fairly high for the GTO (several hundred mA) and thus it is important to ensure that the latching current has been exceeded before cutting off the gate current, especially if fast turn on networks are used (capacitance + resistance + inductance), particularly with inductive loads.

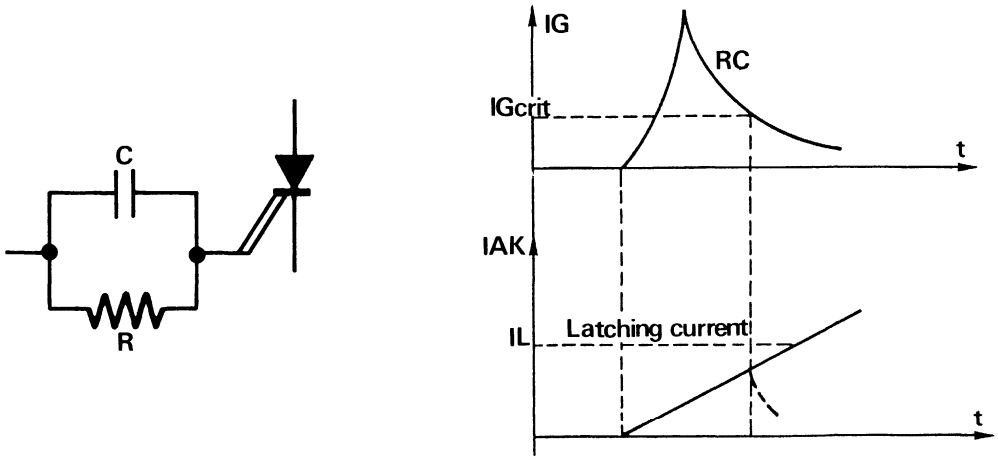


Figure 2-233 – Turn on conditions

Fast turn on is necessary to reduce losses in as the following figures describe.

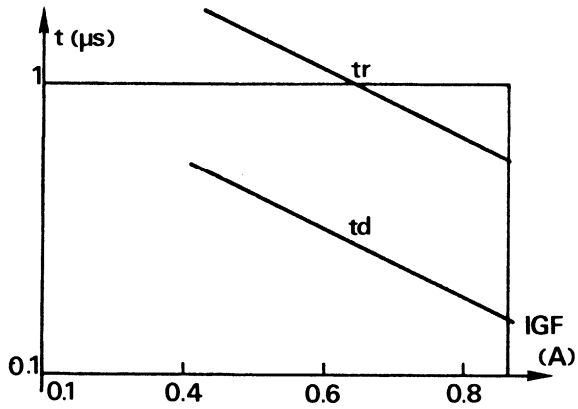


Figure 2-234 – Turn on time = f(IG)

J-7. Turn on currents/voltages

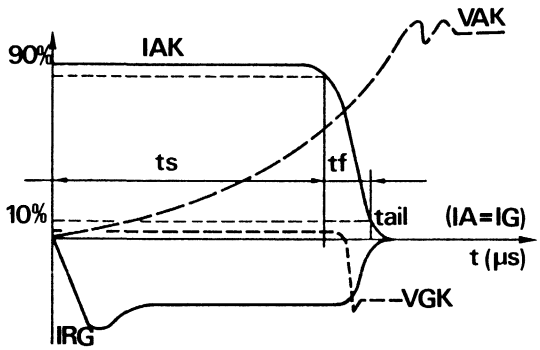


Figure 2-235 – Turn on waveforms the effect of gate control on turn off times

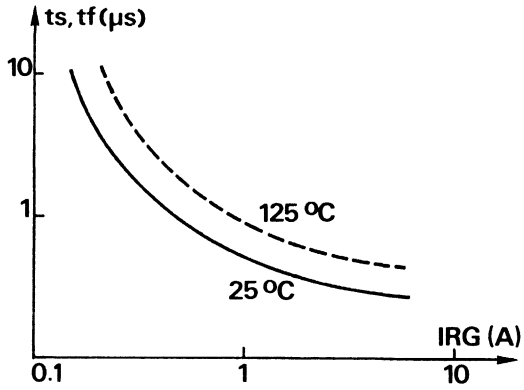


Figure 2-236 – Turn off time = f(IRG)

The gain at turn off is also a function of the junction temperature.

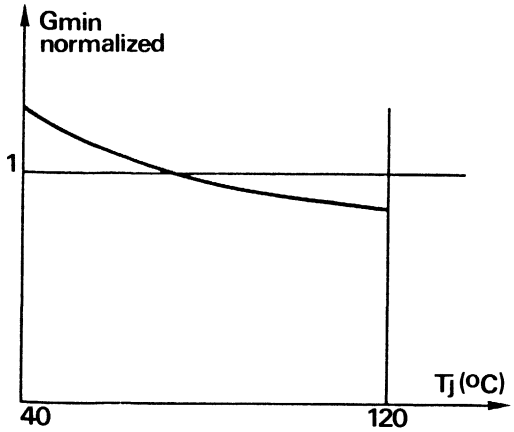


Figure 2-237 – Minimum gain in relation to junction temperature

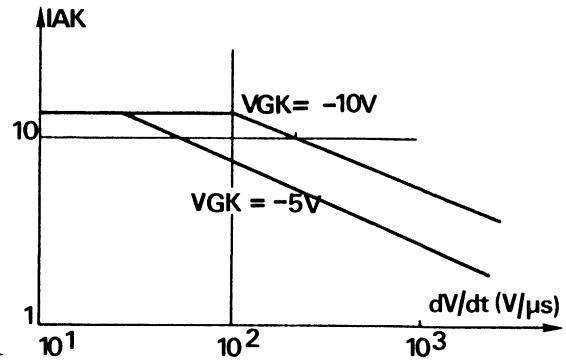


Figure 2-238 – Reapplied dV/dt = f(IAK) VGK

GTOs have a maximum dV/dt which must be respected at turn off, this also relates to the anode current before turn off and the gate bias at the moment of turn off.

K) The ASCR asymmetric thyristor

Continuing technological improvements on SCRs have resulted in: reducing the tq, thus increasing operating frequency, increasing the forward current density through efficient use of silicon, reducing on voltage VT and thus reduce on losses, but to the detriment of reverse blocking voltage, hence the name asymmetrics SCR. This is not of great importance as for most applications, a reverse current is passed through an anti-parallel diode.

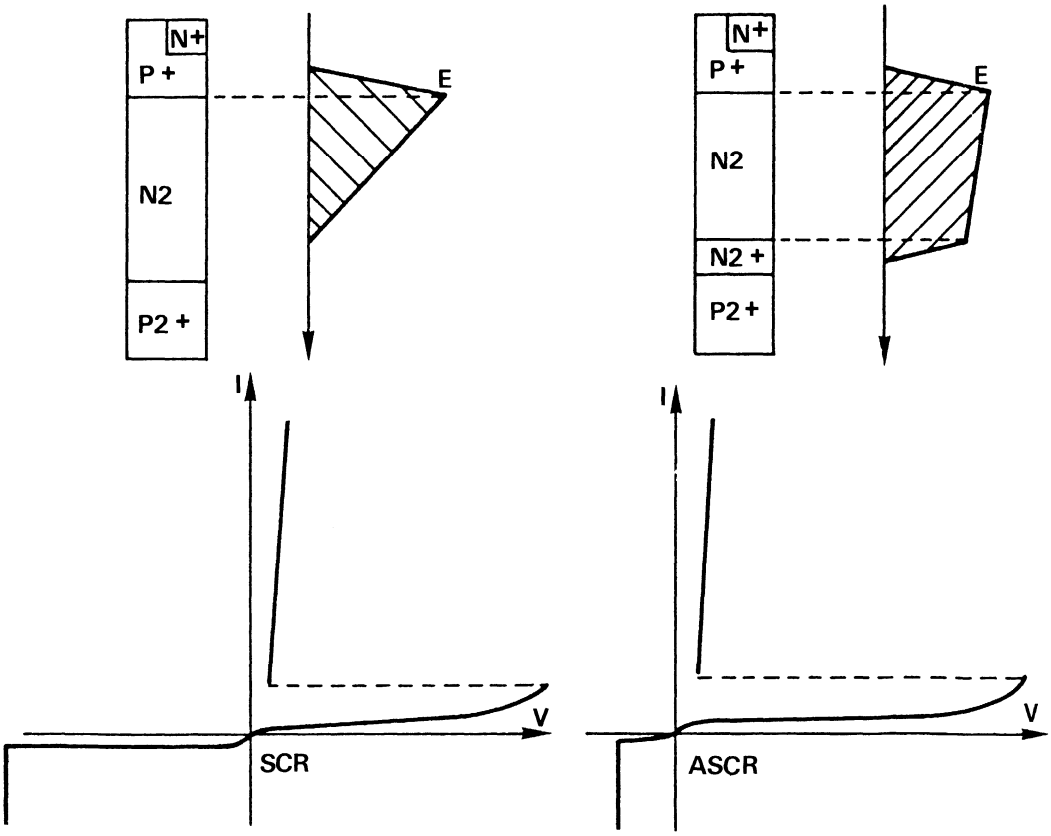


Figure 2-239 – Comparison between a classic SCR and an ASCR

In the ASCR, a highly doped layer is added at junction N2 P2 with the aim of stopping the extension of the electric field cross hatched portion of Figure 2-239. For the same VDM and N2, tq and switching losses may be reduced without increasing on losses.

The disadvantage of this N2 layer is that it reduces the structure's reverse blocking voltage (VRRM) by some 20 or 30 V. If the application requires an increased reverse blocking voltage (rare occurence), a diode may be added in series.

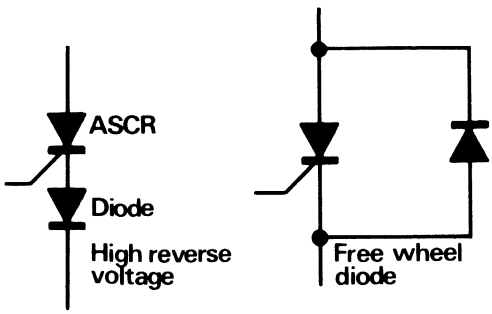


Figure 2-240 – Possible uses of the ASCR

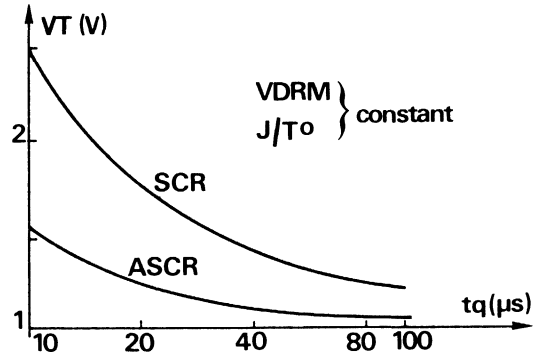


Figure 2-241 – On voltage in relations to the technology

ASCR on losses may be shown compared with the classic SCR in terms of forward voltage versus tq.

This results in the curves of efficiency (power loss) of the two devics as a function of frequency.

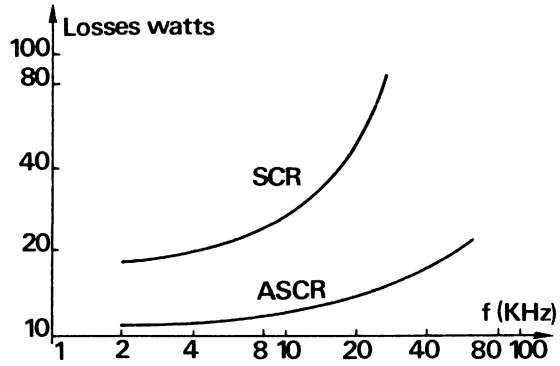


Figure 2-242 – Losses in terms of frequency

L) Trigger devices

L-1. The unijunction transistor (UJT)

L-1.1. THEORY

A UJT is a device with 3 terminals: emitter, base 1 and base 2. The unijunction transistor (UJT), a double base diode, has just one PN junction. It is usually classified with the SCRs (3 junctions) as they are very often used together.

It can be represented by a type N silicon bar with high resistivity when VB2-B1 is applied between the bases, the result current is: IB2B1 = VB2B1/RBB.

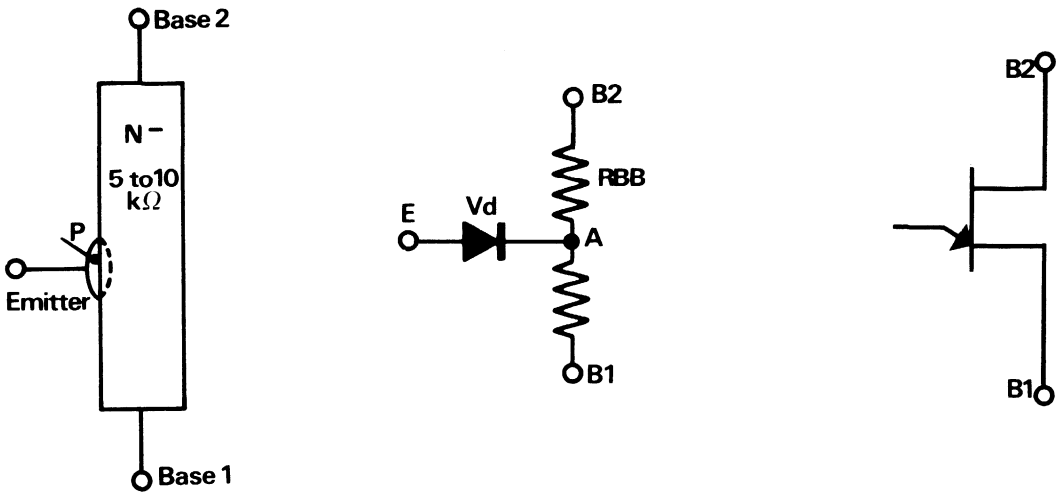


Figure 2-243 – Representation of UJT

With IB2B1 current flowing the voltage at point A becomes:

$VA = \eta\ VB2B1$

η being called the intrinsic standoff ratio, it varies from 0.5 to 0.8. To forward bias junction EB1, voltage would be needed of:

$VE = VD + \eta\ VB2B1 = Vpeak\ (1)$

VD being the diode voltage drop, with approximately 0.5 V at 25°C.

When the junction is forward biased, the holes are injected into the silicon bar and move towards B1 because of the electrical field.

Electrons are also injected but in the opposite direction by base 1 to maintain equal charge. Thus the resistivity between the emitter and base 1 decreases. VAB1 also decreases which improves the efficiency of the hole injection. Resistivity reduces even more and soon.

In this way, conductivity modulation and a negative resistance region result. The limit is fixed by the saturation of hole concentration in the silicon of about 10^{16} carriers/cm^3.

The point where RB1 reaches a minimum (from 5 to 20 ohms) is a valley, hence the valley voltage current.

The saturation region is entered with a fixed resistance, resulting in $VEB1\ sat = K\ I_E$.

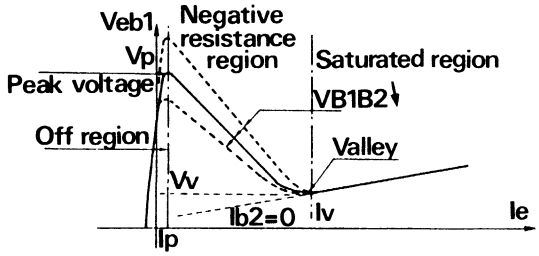


Figure 2-244 – Characteristics of UJT emitter (not to scale)

If VBB = 0 (IB2 = 0) a diode junction characteristic results when VB2B1 varies, Vpeak also varies.

L-1.2. STATIC CHARACTERISTICS

A = V_E = F(IE)

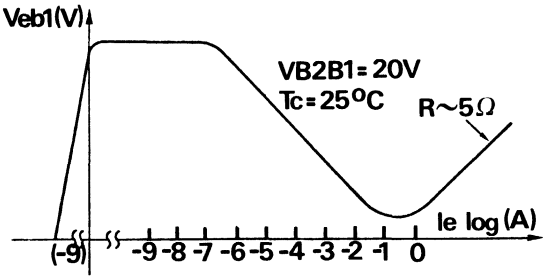


Figure 2-245 – Emitter-base 1 characteristics of UJT

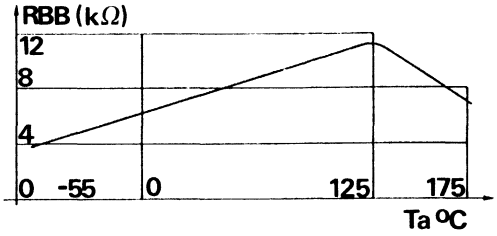


Figure 2-246 – rbb = F(T°C)

Diode V_D voltage drop, VD depends, as in a classic diode, on the current which passes through it and the temperature.

For a peak current Ip = 1uA, $V_{DT} = V_{25} - (T-25)K_D$ (3) with $K_D \cong 2{,}7$ mV/°C.

Intrinsic Standoff Ratio = η, where $\eta = \frac{RB1}{RB2B1} = \frac{Vp-VD}{RB2B1}$

This ratio could be thaught to be independent of temperature. In reality, it becomes slightly lower with increasing temperature in a Kη ratio of about, $K\eta \cong 6\ 10^{-4}$/°C resulting in $\eta T = \eta 25\ (1-(T-25)K\eta)$ (4). Thus η is practically independent of VB2B1.

Interbase RBB resistance

This resistance between bases 1 and 2 is very dependent on the temperature, as shown in Figure 2-246.

Between 0 and 125°C, $R_{BBT°} = R_{BB25}\ (1+(T-25)Kr)$ (5) with $Kr = 8.10^{-3}$/°C. RBB also varies with VB2B1 interbase voltage.

For VBB = 3 V, RBB would be $R_{BBV} = R_{BB}\ (1+(V_{BB}-3)K_V)$ (6) where $K_V \cong 12\ 10^{-3}$

Peak characteristics

Vp decreases with increasing temperature (see formula 1 where VD and η decrease with temperature). This variation can be compensated by adding an external resistance in series with base 2.

From equation (1), $Vp = VD + \frac{\eta\ V1rBB}{(rBB + R2)}$ (7)

When the dVp/dT equation equals zero, R2 becomes:

$$-2R2 = 2RBB + V1\eta\ \frac{Kr}{KD} + V1\ RBB\ \frac{Kn}{KD}$$

$$\pm \left[2RBB + V1\eta\ \frac{Kr}{KD} + V1RBB\ \frac{Kn}{KD} - 4RBB\ (1 + V1\ \frac{Kn}{KD})\right] \quad (8)$$

Taking into account that RBB depends on the supply voltage. Also, RBB and Kr varies with Kη. η also depends on supply and VB1B2 depends on R2 which makes equation 8 unwieldly.

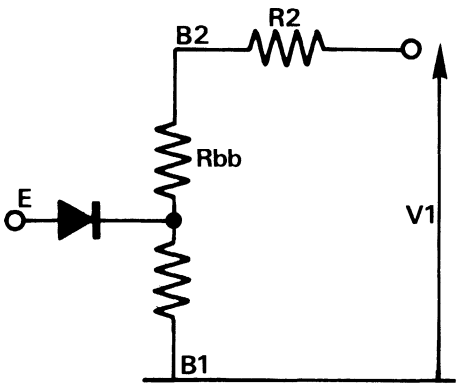


Figure 2-247 – R2 external resistance

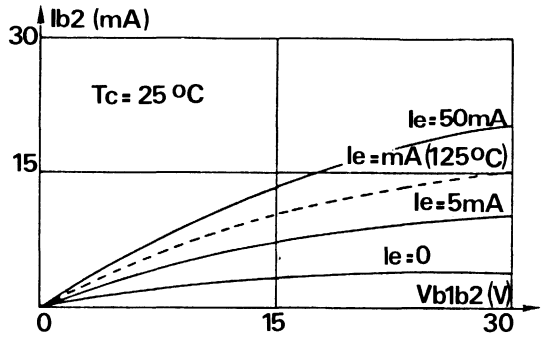


Figure 2-248 – IB2 = F (VB1B2)

From experience, it has been shown that **R2 = .15RBB**

For greater precision, adjustments must be made on the circuit.

Valley characteristics

The valley voltage V_V and valley current I_V decrease with temperature between (-55)and +100°C.

$V_{VT.} = V_{V25.}\ (1 - \beta VT)$ with $\beta V \cong 8\ 10^{-4}$ (very low variation) $I_{VT.} = I_{V25.}\ (1 - \beta IT)$ with $\beta I \cong 7\ 10^{-3}$ these parameters are also dependent on VB1B2, increasing with this voltage.

Thus VV Voltage = VV 10 V (1 + γ V VBB) for VBB between 10 and 30 V with $\gamma V = 6.10^{-3}$ (very small variation), $I_V = I_{V10V}\ (1 + \gamma I\ VBB)$, $\gamma I = 3.10^{-2}$.

IB2 Interbase current

The interbase current increases with increasing VB2B1 supply voltages and emitter current IE but decreases with increasing temperatures as shown in Figure 2-248.

L-1.3. DYNAMIC CHARACTERISTICS

A typical application for a UJT is as a relaxation oscillator described in Figure 2-248.

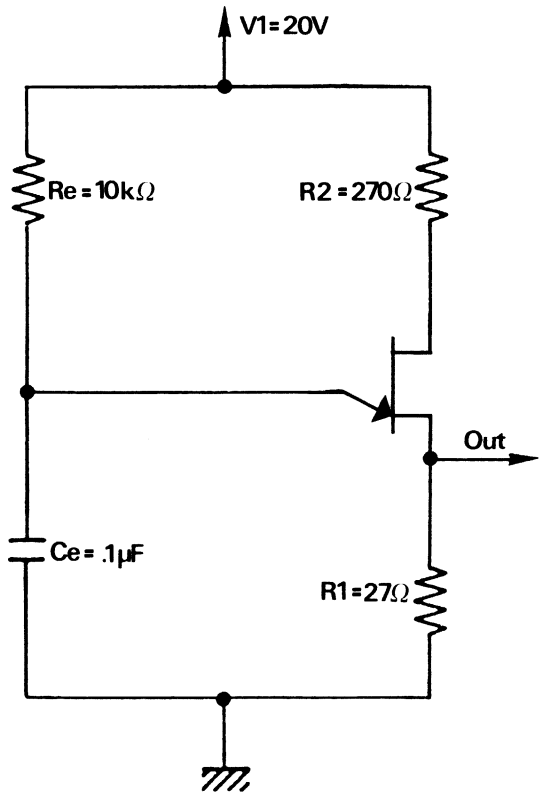


Figure 2-249 – Typical use of the UJT

With this circuit the VR1 rise and fall time of the output pulse is shown in the oscillograms as following:

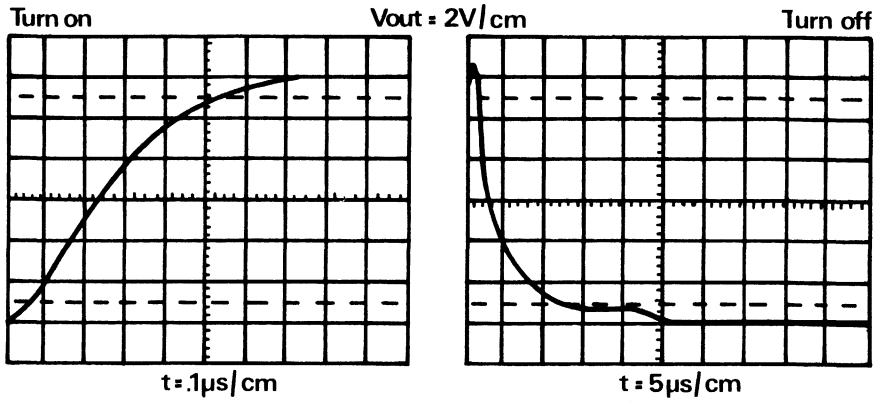


Figure 2-250 – Switching oscillograms for UJT

The relatively long period of cut off is due to the charging of capacitor Ce. For lower capacitor values, thus time will decrease accordingly.
Thus the value of Ce influences the ton and toff times.

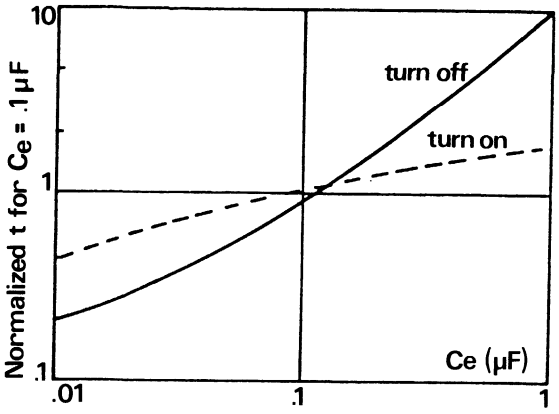


Figure 2-251 – Switching times in relation to Ce

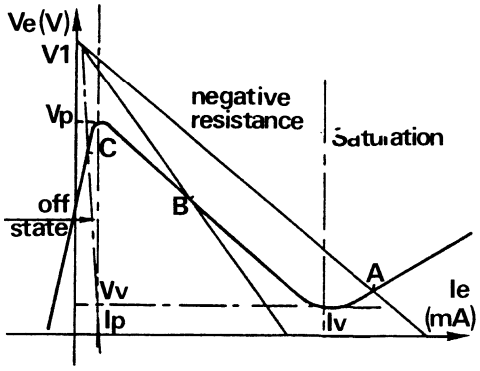


Figure 2-252 – Loadlines

L-1.4. APPLICATION

Relaxation oscillator.

See Figure 2-249. The first criteria for operation is that Re should be low enough to supply Ip (min); i.e.: Remax $= (V1 - VP)/IP$ where V1 is the supply voltage.

If Re is too low, the load line subtends the characteristic at point A and the device latches on, therefore the minimum value of Re is defined as $Re(min) = (V_i - V_V)/I_V$.

At the point when Re is greater than Remin the loadline intersects the negative resistance characteristic at B, and the UJT can oscillate.

The load curve is given in the following figure.

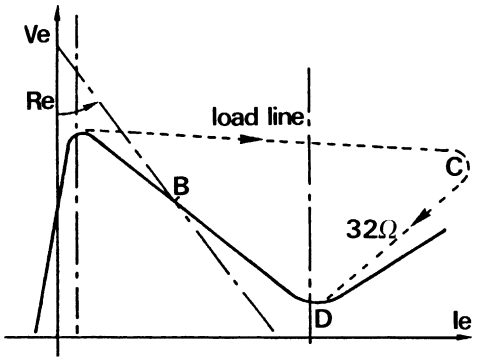


Figure 2-253 – Load line with RC

The previous loadline is valid for Re load resistance. If an RC circuit is used, thus at Vp the condensator to discharge to C in a very short time, then from C to D with a slope of R1 + (R1B1 saturation) in this case, about 32 ohms down to the valley current. At this point the load line retraces to point B, voltage at capacitor C terminals tends to reach V1 but at Vp the system starts up again and so on, with a T period such as T = ReCe Ln $1/(1-\eta)$ + toff (9)

If we take η = 0.63 we have T≅ReCe + toff and if ReCe is great, well above toff, we can say that T≅ReCe.

Long term timer

If long time delays are required (from several minutes to several hours), ReCe has to be increased.

But large capacitors with low leakage currents are expensive, so it is better to increase Re (limited by Re max). For long time delays, it is advantages to charge the capacitor with a constant current, using a JFET, rather than a very large Re (Figure 2-254).

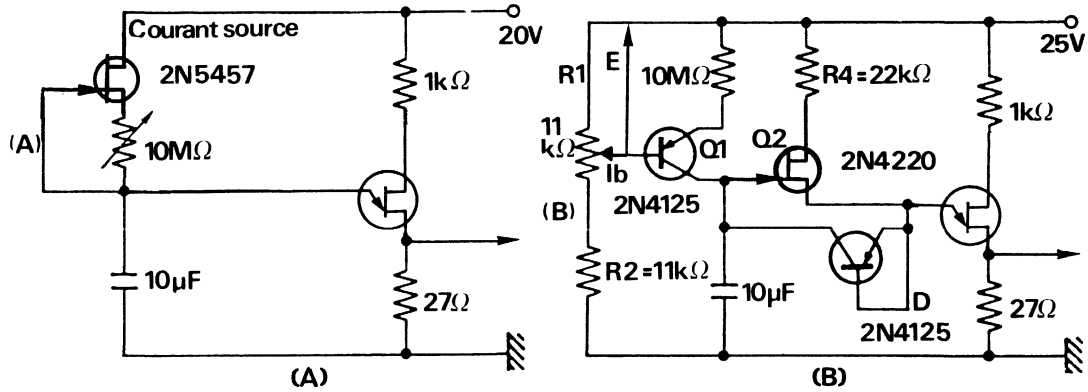


Figure 2-254 – Long term timer

With the circuit of Figure 2-254 (a), 1µA of load current can be readily obtained hence

delay times of $t = \frac{(Vp - Vv)\,Ce}{I\,load}$

If Ce is in µF and I in µA, t is, in seconds. With Vp = Vv = 10 V and Ce = 10 µF, t = 100 seconds. With the circuit of Figure 2-254b, much longer times can be obtained by separating the loadcurrent It. Q1 R1 R2 and R3 are the current source which can supply several nanoamperes.

The capacity load is given by: Iload = $\frac{E - VBE}{R3}$ - IB. IB being very small, Iload can be regulated, thus t is proportional to R3. UJT emitter current IE is controlled by the JFET Q2 and limited by R4 to give an IE between IV and Ip.

Periods of up to 10 hours can be obtained by using this circuit.

L-2. The programmable unijunction transistor (PUT)

L-2.1. THEORY

This is a 4-layer device similar to an SCR, but unlike the usual method of control of the lower junction (NPN composite transistor base) here it is the upper junction (PNP composite transistor base) where the gate lead for control is brought out.

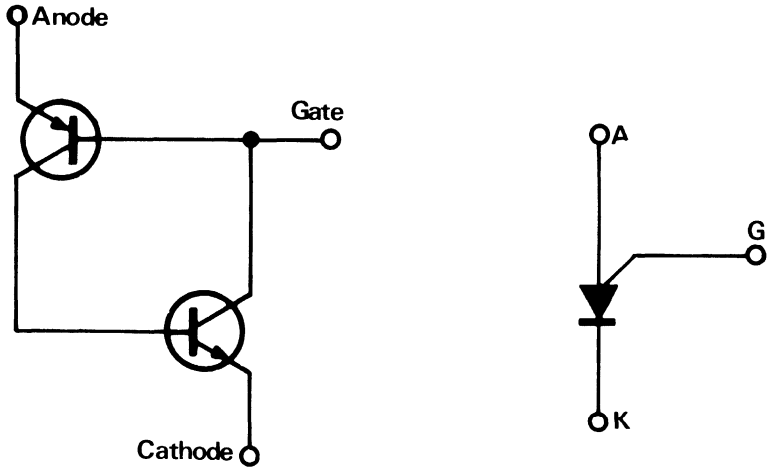


Figure 2-255 – The symbol and the equivalent circuit of a PUT

L-2.2. OPERATION

The PUT is similar to a UJT but here the control voltage is programmed externally by a resistance network.

The PUT is more sensitive, faster, more versatile and generally more economical than a UJT and often replaces it. The UJT has the advantage of allowing great variation in operating frequency.

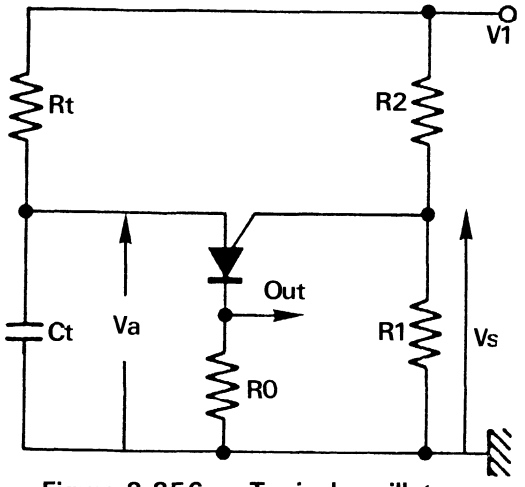


Figure 2-256 – Typical oscillator configuration

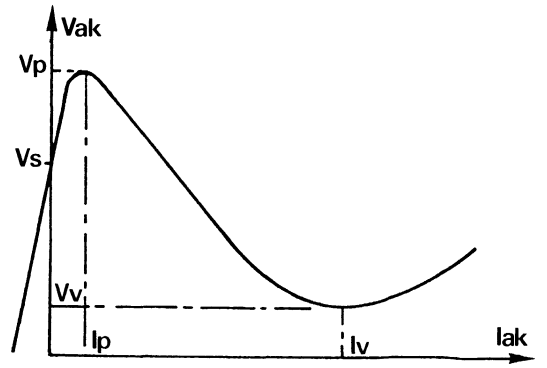


Figure 2-257 – Characteristic VAK: f(IAK)

How this device operates in a relaxation oscillator identical to the one used for the UJT will now be examined.
By using the circuit of Figure 2-256 it is apparent that the PUT will fire when $V_A > V_S$ by a diode junction drop of about 0.5 V.

Since Vs is programmed externally, VA is then also programmed (known as Vpeak if UJT terminology is used).

The emitter characteristics is similar to that of the UJT with its negative resistance region. Thus, if IAK is above IV we have a stable state. If Rt is such that it cuts the characteristic in the negative resistance region, we have a relaxation oscillator, Figure 2-257.

L-2.3. DYNAMIC CHARACTERISTIC

By using a capacitor of 1000 pF, turn on times in the order of 40 ns will result. The period is defined by $T = R_T C_T \text{Ln} (I + R1/R2)$.

The minimum value of resistance to give maximum oscillation frequency is:
$R_{mn} = 2 (V1 - Vv)/Iv$ with Vv often being negligeable. For minimum frequency, it is better to increase CT to 10 μF using a very low leakage current capacitor (Mylar). Thus, $R_{max} = (V1 - Vp)/2Ip$. A put can operate at from frequencies 0.003 Hz to 2 KHz.

L-2.4. TEMPERATURE COMPENSATION

For the circuit of the Figure 2-256 with variable ambient temperation, the oscillation frequency can vary from 2 to 3% between 25 and 60°C, especially for low frequencies.

Several forms of compensation are shown below:

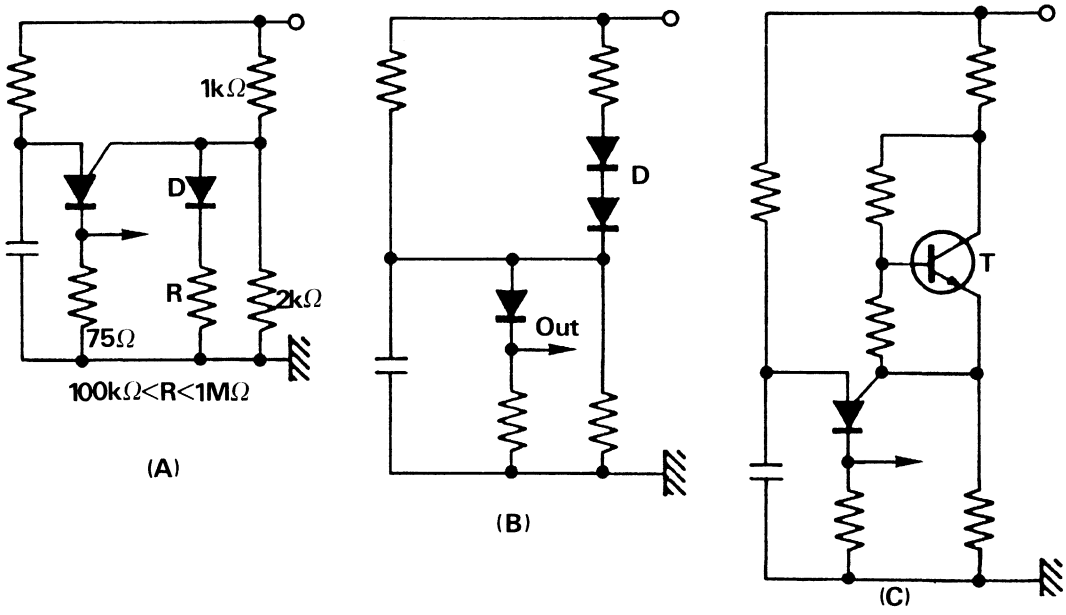


Figure 2-258 – Various temperature compensation networks

The negative temperature coefficient of the VAG is mainly responsible for the increase in frequency when the temperature increases.

So Vs must be increased when the temperature increases to keep a constant frequency.
For this, in the circuit of Figure 2-258a, diode D is based so that VD increases with increasing temperature.
In circuit 2-258b, the VD voltage decreases with increasing temperature. For circuit 2-258c, transistor bias is controlled so that VCE reduces with temperature.

L-2.5. APPLICATION

Identical to that of the UJT, but often easier to understand, the UJT even more than the PUT can work at very low supply voltages as the VAK of a PUT can be 1.5 V while for a UJT it is 3 V. Like the UJT, for very long relaxation times, a constant current derived from a JFET can be used.

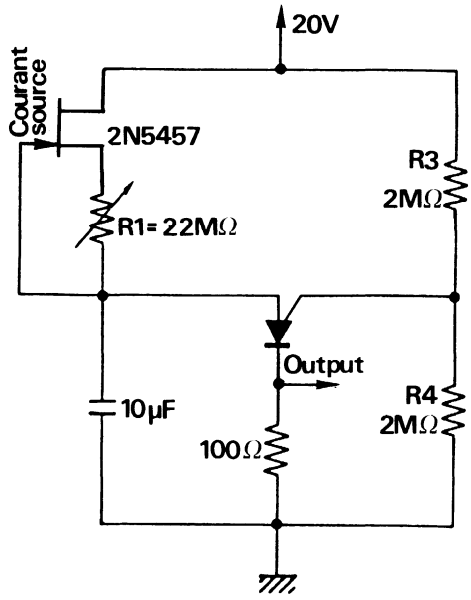


Figure 2-259 – 20 minute impulsion

R1 is adjusted to VGS/Io with VGS = Vp (1 - $\sqrt{Io/IDSS}$)
Io being the constant current source.
Vp is JFET pinch-off voltage.
VGS gate source voltage.
IDSS current drain source with the gate short circuited at source.
Thus the period becomes T = CΔV/I in seconds.
C capacity in microfarad, ΔV voltage variation on C and, I load current of C.
The maximum period is limited by the Ip peak current to fire the PUT. In this way, this device can obtain longer periods than the UJT because it has a lower peak current and can be reduced to minimum by raising RG to maximum.
(RG = R3/R4, equivalent parallel network: Thevenin's Theorem). Ra = R3R4/(R3 + R4) = 1MΩ. VS = Vp - VAG = V1 R4/(R3 + R4).

L-3. Diac bilateral trigger diode

L-3.1. THEORY

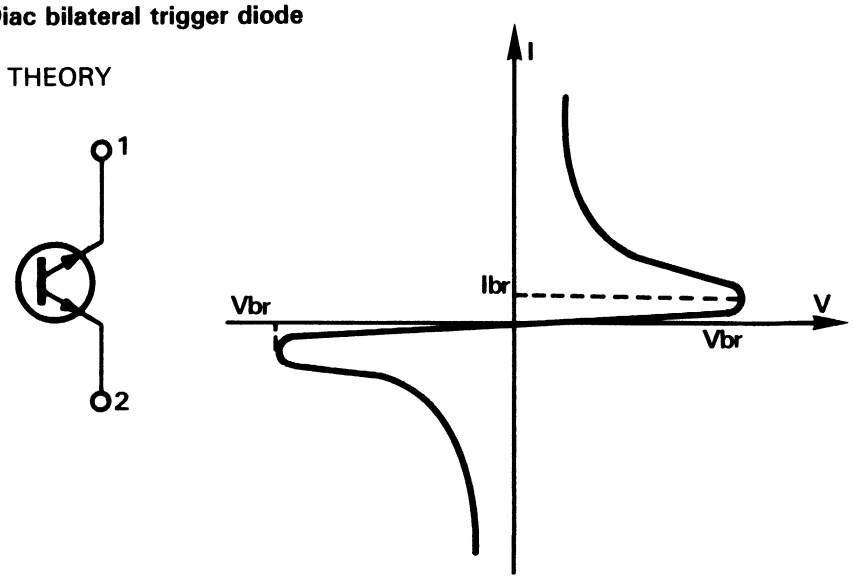


Figure 2-260 – Symbol and static characteristic

Basically, a DIAC is an open base transistor with identical doping at both junctions.

The symbol and output characteristics are shown is Figure 2-260 . As in all trigger devices, the DIAC is characterized by a negative resistance region.

L-3.2. CHARACTERISTICS AND APPLICATION

Breakdown voltage is generally fairly low (20 . 30 V); IBR current is several hundred microamperes.

The trigger is normally used as in a triac or thyristor control network, for heating, lighting, and motor control, etc.

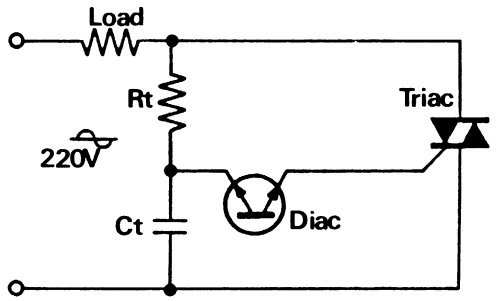


Figure 2-261 – Normal application

L-4. The Sidac, the medium voltage alternative interrupter

L-4.1. THEORY

The sidac is a bilateral switch, operating at medium voltage (240 V max at present) it triggers when the voltage at its terminal exceeds the specified value: Figure 2-262.

This is a semiconductor with two terminals and four semiconducting layers (3 junctions). The symmetrical characteristics shown in Figure 2-263, reaches the breakdown voltage VBO, passes through a negative resistance to the low voltage, saturated state.

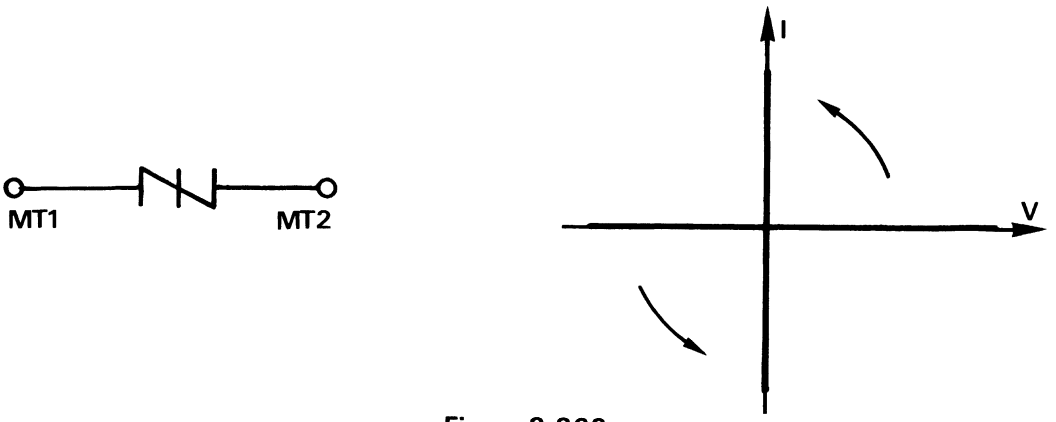


Figure 2-262

I_{RMS} = 1A
I_{TSM} = 20A
I_H = 100mA
$R\theta J$ = 15°C/W
$R\theta JA$ = 45°C/W
DI/DT ≦ 50A/μs
tq ≅ 1μs
Tjmax = 125°C

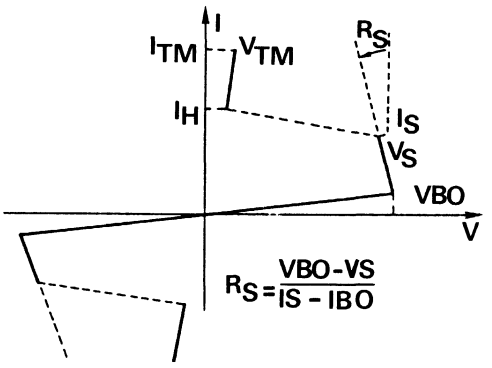
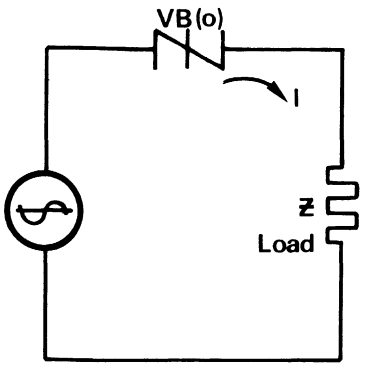


Figure 2-263 – Sidac characteristic

L-4.2. BASIC CIRCUIT



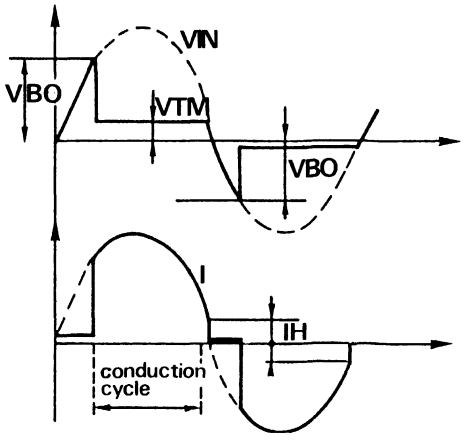


Figure 2-264 – Basic circuit and waveforms

L-4.3. SURGE CURRENT CHARACTERISTICS

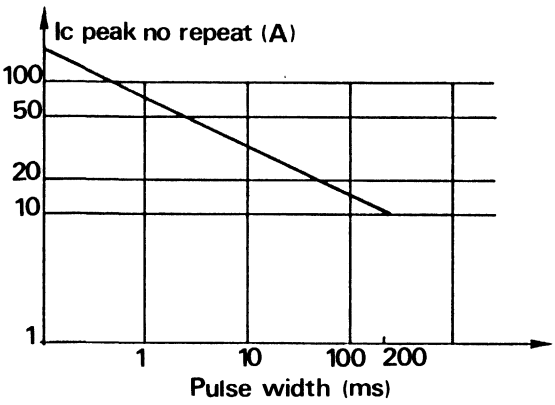


Figure 2-265

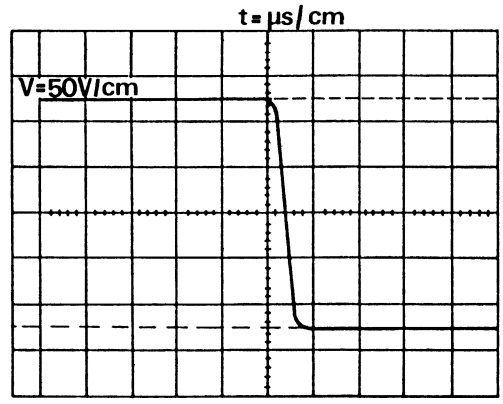


Figure 2-267 – Variable load

L-4.4. APPLICATION

This semi-conductor which operates by voltage like an anode firing thyristor, is very rugged.

It can stand non-repetitive peak current of 200 A for 10 microseconds and can very economically replace a triac and a diac as shown in Figure 2-266.

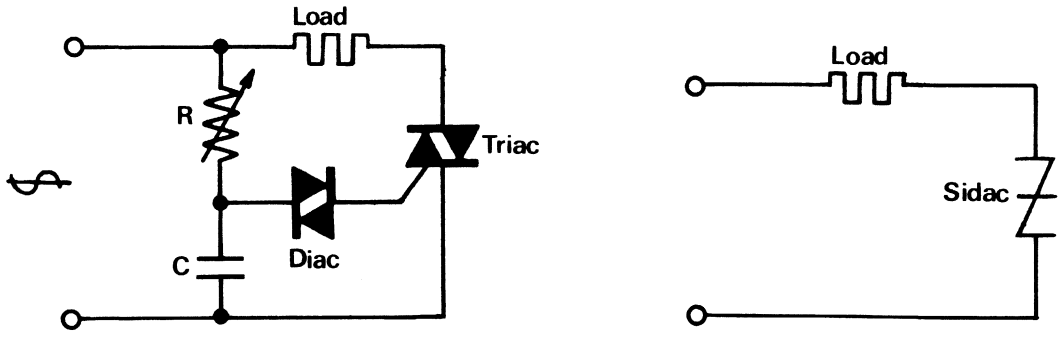


Figure 2-266 – Turn on oscillogram

The Sidac has a relatively close tolerance of ± V_{BO} which makes it useful for protection against overvoltage transients. This device is often more economical than using back-to-back zeners or slower MOV. It can also be used as an overvoltage protection (OVP) on DC power supplies with the addition of a fast fuse. Because of its negative resistance, it can also be used in a very economical relaxation oscillator.

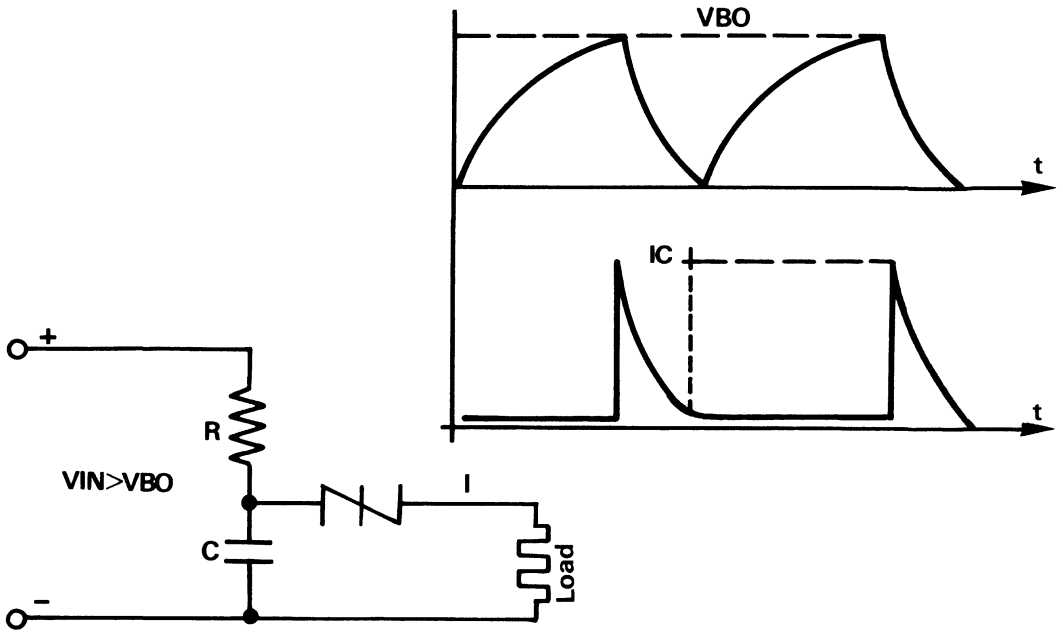


Figure 2-268 – Relaxation oscillator

L-4.5. APPLICATION EXAMPLE: PROTECTION

For the new semiconductor telephone circuits (SLIC: Subscriber, Loop, Interface Circuit).

Voltage surges above 1000 V (lightning induced transients) are suppressed by a gas discharge tube. Voltage surges below 1000 V (positive or negative) are short-circuited by two SIDACS and two diodes in series.

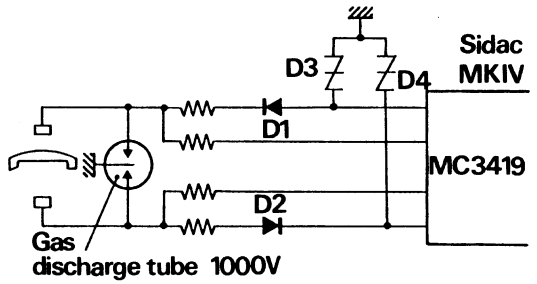


Figure 2-269 – SLIC

L-4.6. APPLICATION EXAMPLE: FLUORESCENT BALLAST

To turn on a low power (20 W) fluorescent tube of short length (20 cm), a breakdown voltage of 250 – 300 V is required. Two series connected Sidacs MK 1 V 140 V for 200 V line operation (300 V max) are sufficient to light the tube as shown in Figure 2-270. Once it is turned on the voltage at terminals is no longer sufficient to restart the SIDACS.

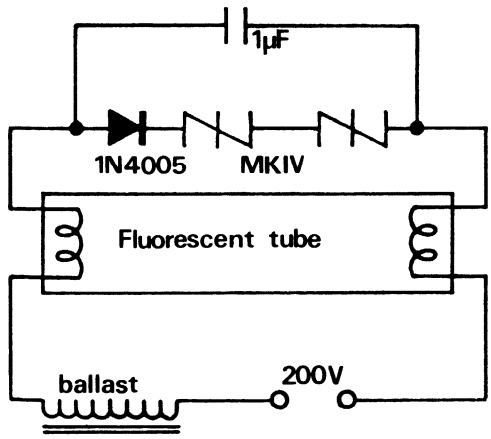


Figure 2-270 – Fluorescent tube starter

L-4.7. APPLICATION EXAMPLE: CAPACITOR DISCHARGE IGNITION

For small combustion motors such as in lawnovers, chainsaws, etc., the Sidac can readly be used as in the capacitor discharge ignition circuit shown in Figure 2-271. In this circuit, the energy is stored and dumped from capacitor to produce the high voltage spark that is synchronized with the magnetic control circuit.

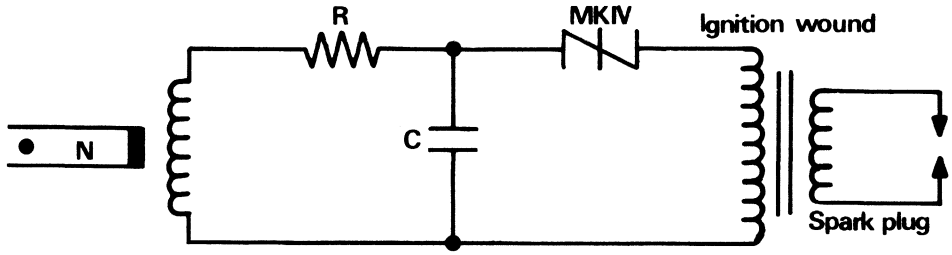


Figure 2-271 – Ignition for small motors

Other similar circuits are:

- to ignite heaters or gas/fuel fired immersion heaters
- not too vigorous for gas

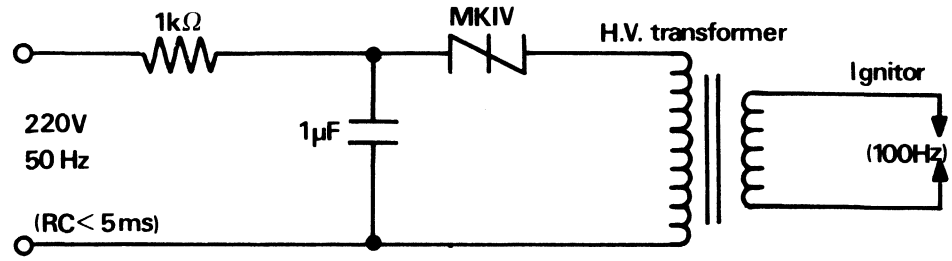


Figure 2-272 – Gas ignitor

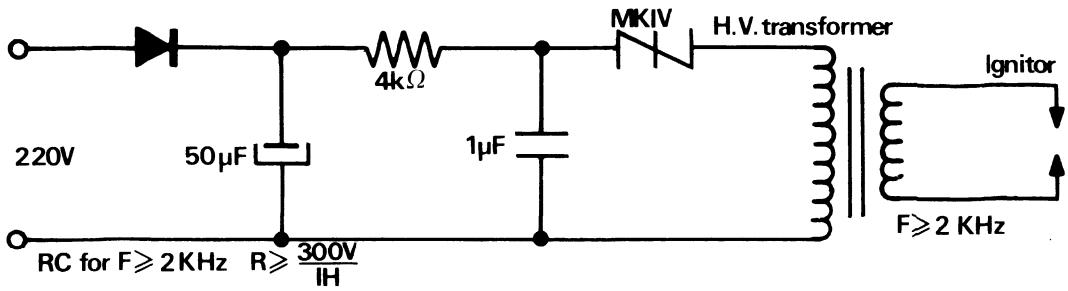


Figure 2-273 – Fuel ignitor

L-4.8. CONCLUSION

In conclusion, for inexpensive applications such as:

- protection against overvoltages,
- high voltage triggers
- relaxation oscillator
- energy regulator

The SIDAC has a bright future especially:

- for telephone – communication or in the automobile applications
- for ignition of gas mixtures (combustion engines, heaters, gas tubes etc.)
- for overvoltage protection
- for all bidirectional triggering, thanks to its ruggedness low cost and simple operation.

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Note interne.

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15 – AN294: UJT applications.

16 – AN413: UJT trigger circuits for thyristors.

17 – AN527: PUT theory and applications.

Environment networks of bipolar transistors

Section 3

TABLE OF CONTENTS

1. Base control of power transistors

A) Introduction

For several years the power transistor was used primarily as an amplifier. It was used in its active zone where the output current is proportional to the input current.

At the same time the need became clear for an ideal switch:

- infinite impedance at opening
- zero impedance at closing
- control which is simple but noiseproof
- rapid turn-on and turn-off transitions
- high long-term reliability

If the electromechanical relays respond well enough to the first 3 conditions they are far from ideal for the last,despite numerous technological improvements (mercury contact, vacuum etc). Today's power transistor can reasonably meet all these needs.

B) Analysis of physical phenomena of switching

If we trace the Ic vs Vce characteristic of a high voltage transistor connected in a common emitter configuration, we see that these curves reveal an area which is not apparent in low voltage power transistors: quasi saturation.

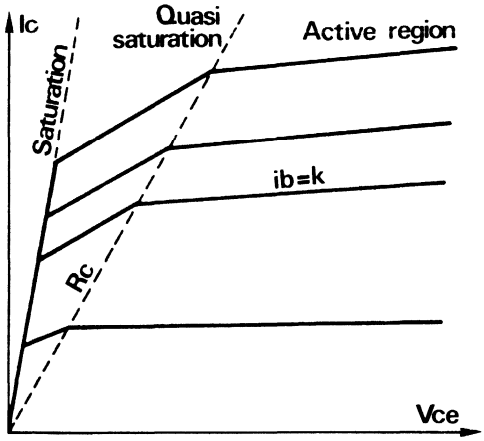


Figure 3-1 — H.V. Transistor Icx Vce

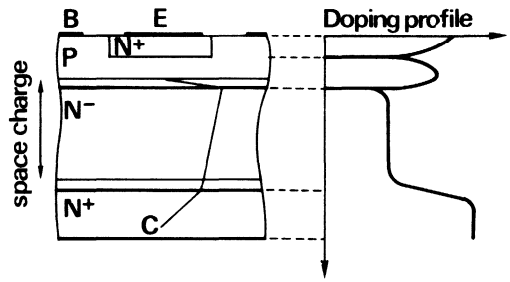


Figure 3-2 — H.V. Transistor structure

To understand this phenomenon particular to high voltage power transistors, it is useful to show the cross section of an emitter finger.

We can see a collector region which is very lightly doped. The light doping is required for high breakdown voltage, but comes with a trade off, high collector resistivity.

For the typical high voltage power transistor, resistivity (ρ) is on the order of 100 Ω-cm, giving a zone which is highly resistive in series with the collector.

It is this resistance which gives the slope to the quasi saturation graph.

We will now study what takes place in this structure during switch-on.

First, certain parameters remain to be defined. For this, imagine an ideal pulse-generator, connected at the base of the power transistor. We have thus the following oscillogram.

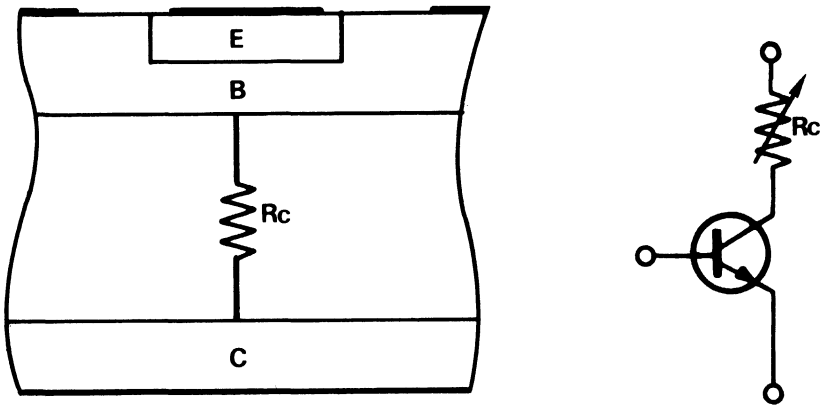


Figure 3-3 — H.V. Transistor collector resistance

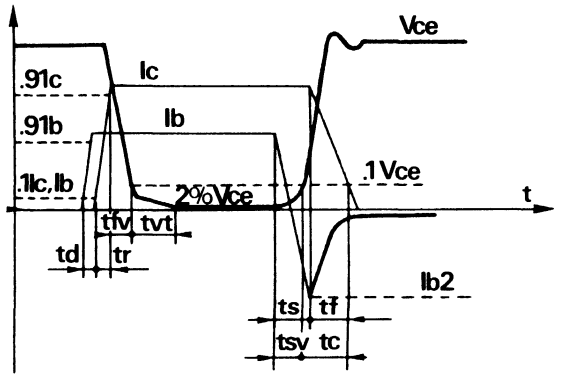


Figure 3-4 — On inductive load

B-1. For turn-on

Before the turn-on transition the transistor is assumed to be blocked with a base polarisation of zero or negative (VBE off).

B-1.1. DELAY TIME (td)

As soon as base current is applied, the holes move from the base towards the emitter and the electrons in inverse direction from the emitter to the base since the emitter has a level of impurities (dopage) greater than that of the base, the electron current is greater than that of the holes, and passes easily through the relatively thin base, to be collected by the collector.

Before this can happen, however, the space charge regions within the transistor have to adjust to the new bias condition. This process takes a finite amount of time, called delay time, and is commonly modeled with the electrical analog in Figure 3-5.

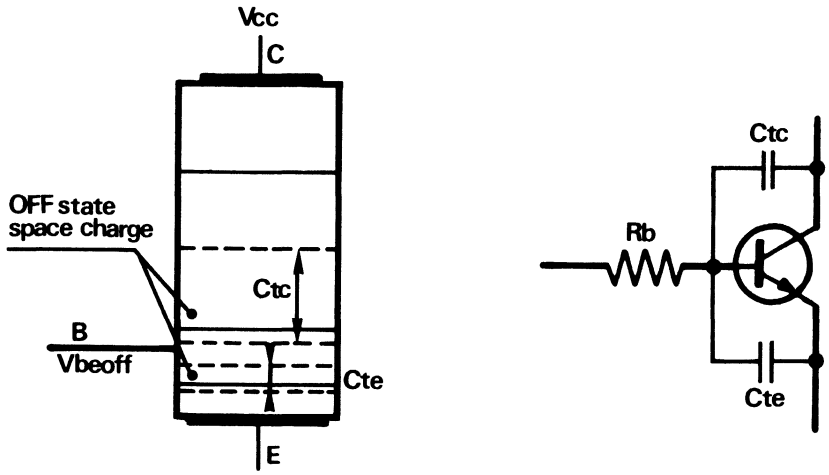


Figure 3-5 — Transistor internal capacitance

B-1.2. RISING TIME, LINEAR ZONE (tr)

From this point on load current is a function of base drive. There are three constraints on base drive at this point, if must:

- compensate the recombination of the carriers
- charge the capacities varying with the transistor and collector base voltages
- allow the increase of Ic

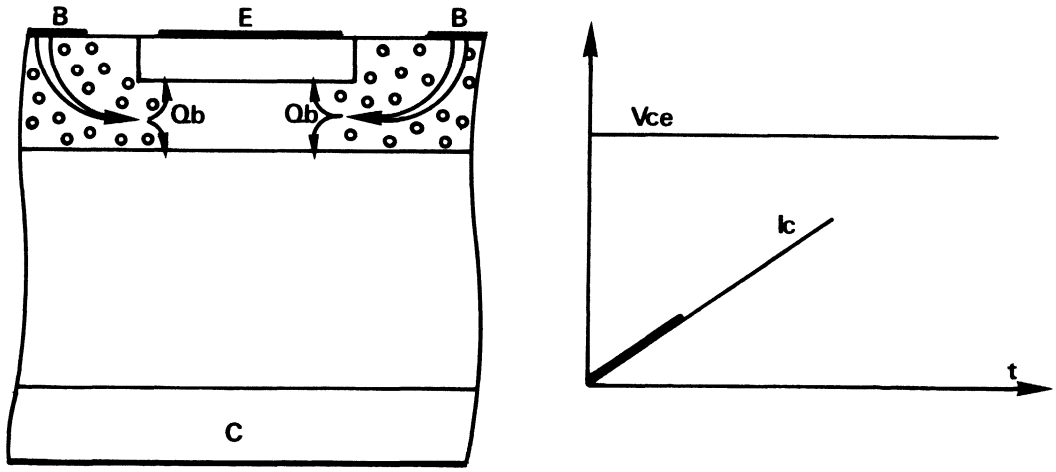


Figure 3-6 — Beginning of conduction

This type of operation restricts conduction primarily to the periphery of the emittor nearest the base contact. In addition, since the base of a high voltage transistor is relatively resistive, the base current creates an electric field which defocalises the current lines.

Bipolar power transistor generally switch through the active region (until quasi sat is reached) quite rapidly. With applied dIb1/dt on the order of 500Amps per µsec, turn-on time is limited primarily by parasitic circuit inductances.

Since R_C may reach 3 or 4 Ω, say for a 10A product, the limit of quasi saturation for a high voltage transistor is fairly high: typically = 30 to 40V

The speed fall in voltage rate at the terminals of the power transistor is very rapid in the order of 30 to 50 ns to discharge the collector-base capacity.

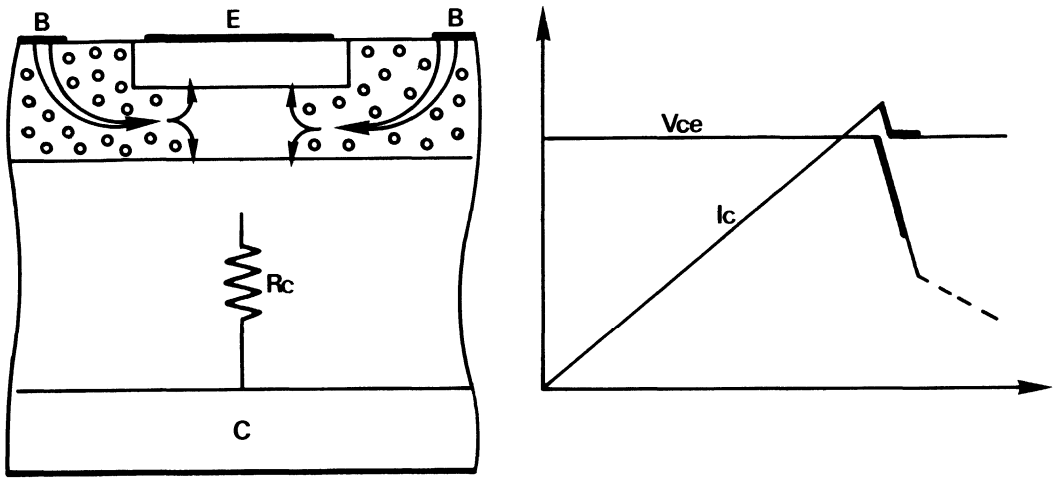


Figure 3-7 — End of current rise

Only the sides of the emitter fingers are engaged in conduction, at turn-on, thereby producing poor utilization of the collector. If the perimeters of the emitter and the base are increased utilization is improved and the turn-on is accelerated: implying a need for products which are highly interdigited.

B-1.3. QUASI SATURATION

When the transistor is switched into quasi saturation, with a forced gain $\beta F = Ic/Ib$, excess holes are brought into the base region.

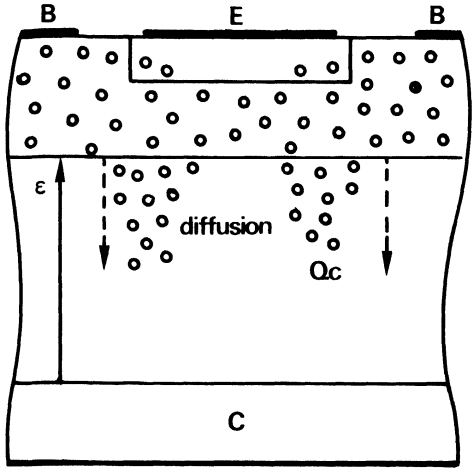
These holes will extend into the base region into the collector, with the extension going deeper into the collector as I_{be} is increased. From an electrical point of view, the base is enlarged, and the collector resistively is reduced by mobile carriers from the base.

The residual electric field in the collector zone due to Vcel (end of linear system) opposes the diffusion of the holes and decreases the speed of dramatically.

This gives even more weight to techniques which reduce Vcel (strong interdigitation).

The excess holes in the base increase artificially Ip, whence the transistor gain diminishes.

If we trace the curve HFE = f(Ic), point Io indicates the start of quasi-saturation at constant emittor-collector voltage.



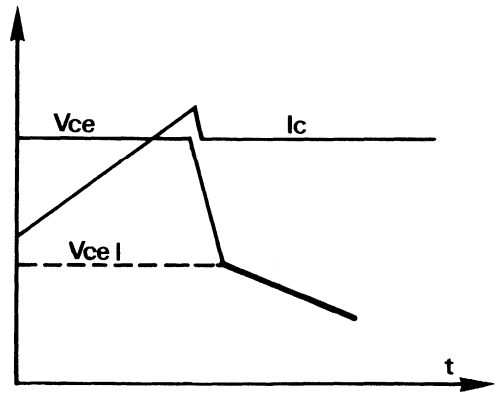


Figure 3-8 — Quasi saturation

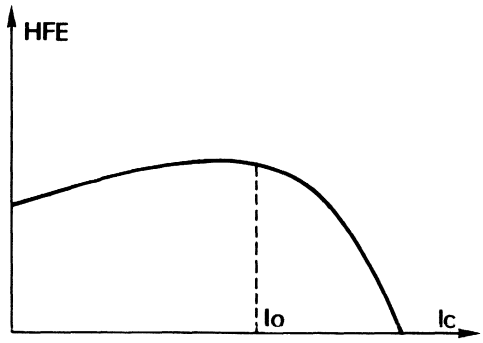
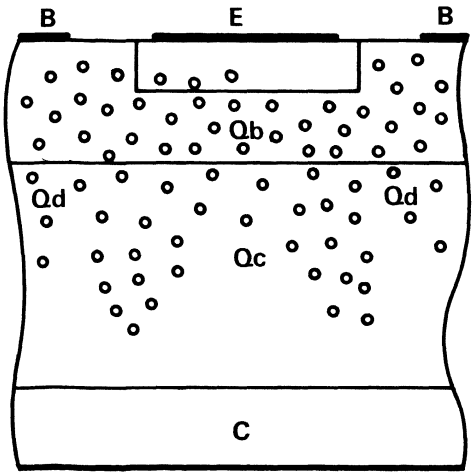


Figure 3-9 — Beginning of quasi saturation

B-1.4. HARD SATURATION

If current Ib continues to rise and brings the operating point into the saturated zone, holes diffuse throughout N- zone of the collector, its collector-emitter voltage decreases to hard sat value.



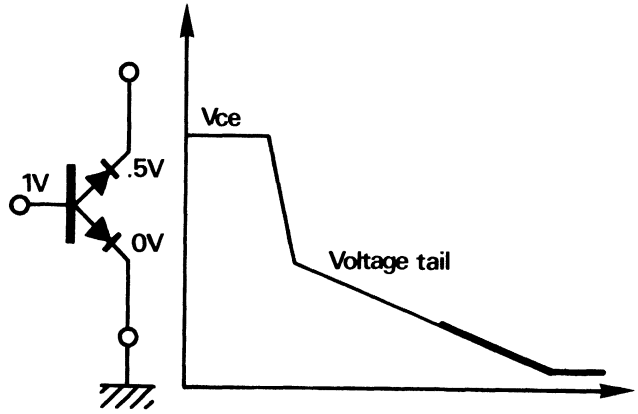


Figure 3-10 — Saturation

If we represent the variation in charge density Qb, Qc and Qd versus Vce and Ic we obtain the following curves.

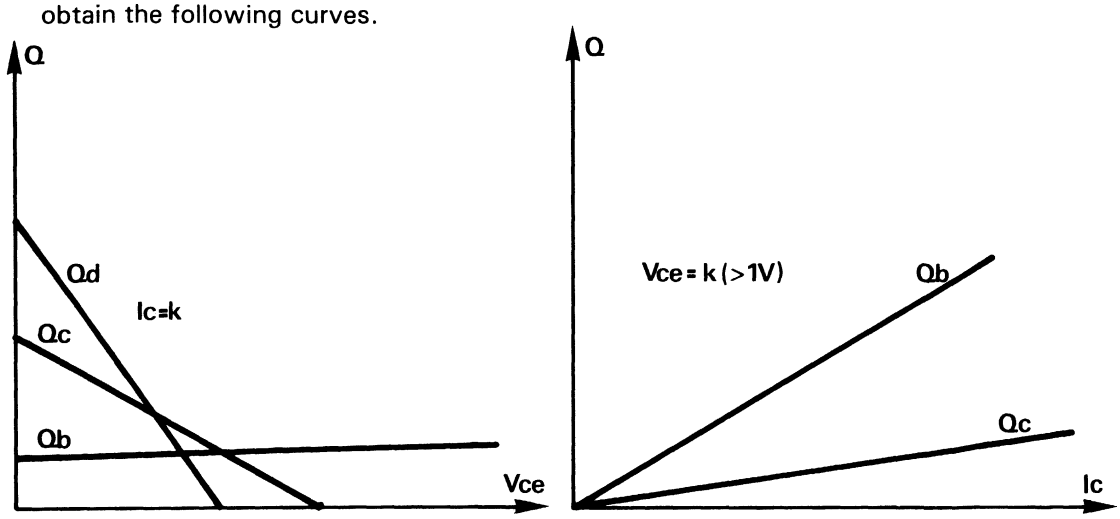


Figure 3-11 — Stored charges versus Ic, Vce

B-2. At turn-off

At the end of the conduction period the current Ib1 is removed and the base is connected to the emitter by a resistance, or else an inverse current is forced into the emitter-base junction (VBE off).

If Ib1 is removed, hole distributions Qd and Qc in the collector tend to move towards the emitter, creating a collector current by maintaining Qb, and producing storage time. The recombination process tends equally to diminish excess holes.

The collector resistance increases producing a rising Vce at the end of the storage period ts. Following this, Qb decreases, Ic decreases, and fall time begins. We then operate in the linear part of curves Ic = F(Vce,Ib). To maintain Ic, Vce increases rapidly and we obtain a long cross over time tc, thus considerable losses.

Reverse base drive will accelerate the disappearance of excess charges, diminishing ts and tf but for classical high voltage technologies, these times are still high as are the losses.

Reverse base drive can be provided by switching the transistor's base to a negative supply voltage. This is a commonly used method of achieving fast transition times and minimizing turn-off losses. We shall study 3 turn-off measurements for this case.

B-2.1. STORAGE TIME

The inverse base current will rapidly extract charges Qd under the base connection.

Then the holes are extracted first from the active region of the collector under the sides of the emitter fingers. Qb and Qc, then appear at the centre of the emitter finger. Ic current is localised here, Rc increases, the active surface area diminishes, and Vce increases. Moreover, as base resistance increases, circulation hole current creates an electric field which further increases current striction at the centre of the emitter finger.

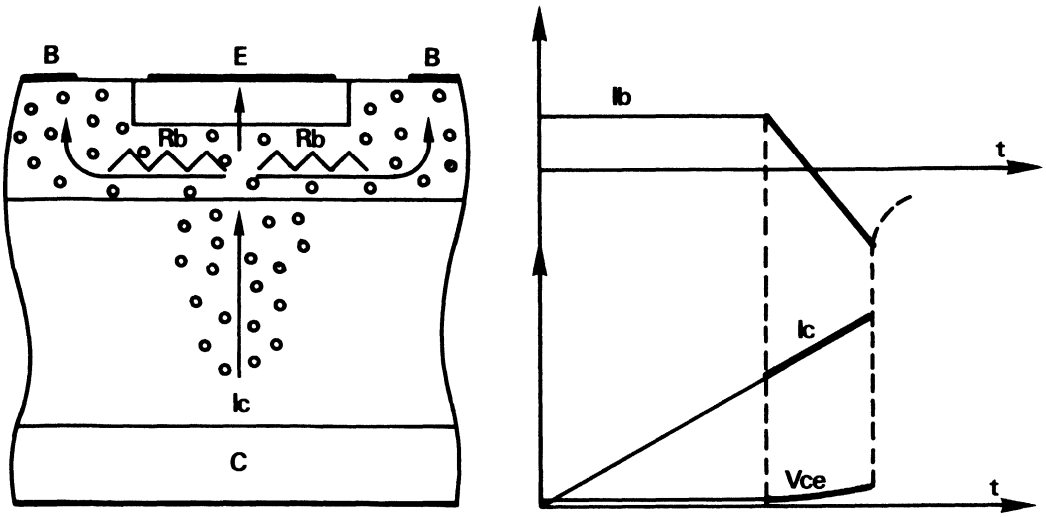


Figure 3-12 — Storage time

B-2.2. CURRENT FALL TIME (VOLTAGE RISE TIME)

When there is only Qb remaining in the base and injection is no longer sufficient to maintain Ic, the collector current decreases rapidly. Collector voltage increases at the same time and this increases the rate of carrier elimination.

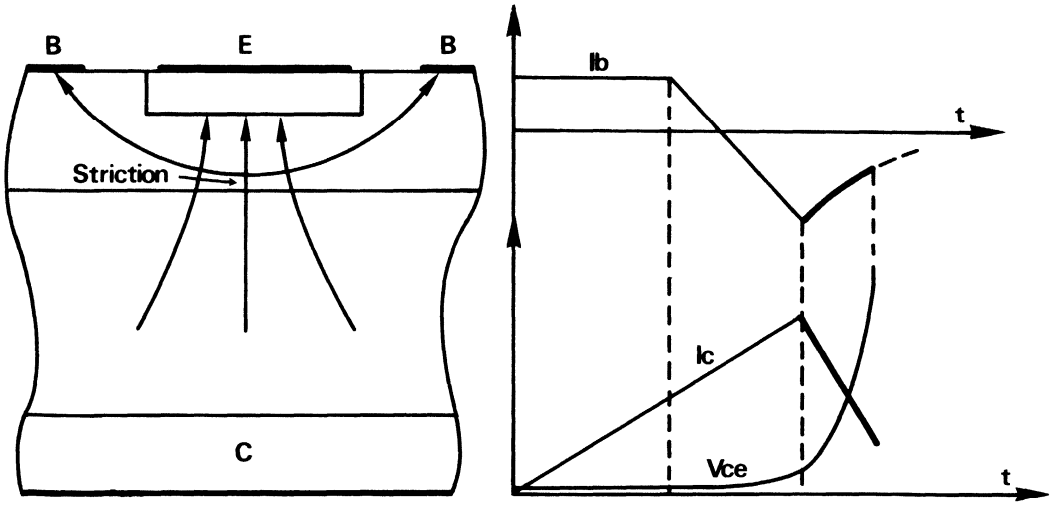


Figure 3-13 — Beginning of turn off

B-2.3. When Qb charges has disappeared, if no rest charge remains, turn-off is complete. Unfortunately in those collector transistors both deep (Wc $\geqq$ 100µm) and resistive ($100 < \rho < 200\ \Omega$ .cm) collector regions a rest charge Qr often remains stored. It can only recombine slowly, leaving is a "tail current" which greatly increases losses.

This phenomenon may have several causes:

- overdrive: too much I_{b1}, produces a large Qr
- rapid extraction of I_{b2}
- insufficient voltage supply which does not sufficiently speed up the carriers remaining at turn-off, therefore a high voltage transistor is relatively slow at low voltage supply
- emitter fingers which are too wide: implies that superior performance is expected from highly interdigitated structures

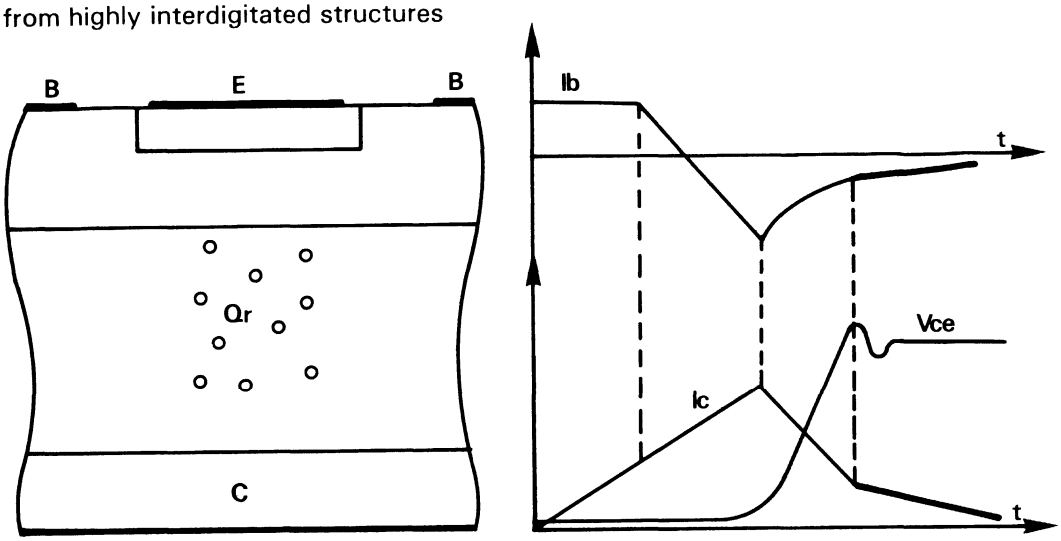


Figure 3-14 – Current tail

C) Switch time equations and interpretation

C-1. Turn on times

C-1.1. DELAY TIME

$$Ib = \frac{dQTE}{dt} + \frac{dQTC}{dt}$$

dQTE/dQTC variations in transition capacitances from the collector and the emitter.

Given that dt = td, we have

$$td = \frac{2}{IB1}\left\{CTe\ VBEOFF^{1/2} + CTc\left[(VCE + VBEOFF)^{1/2} - Vcc^{1/2}\right]\right\}$$

CTe/CTc emitter and collector transition capacities, Vcc = voltage supply, VBEoff = base reverse bias.

We can see immediately that if the transistor is not blocked by a VBEoff just before turn-on, td is negligeable.

If Vce > VBEoff, which is the case for high voltage power transistors, the transistor capacity alone comes into play and $td = \frac{k}{IB1} (VBEOFF)^{1/2}$ (1)

To obtain minimum td, strong Ib1 is required.

C-1.2. RISING CURRENT TIME

$tr = HFE \left(\frac{1}{\omega T} + 1{,}7RC_{TC}\right) Ln \frac{HFE\ IB1}{HFE\ IB1 - 0{,}9\ I_C}$ (2) ωT = turn-off transition frequency.

From this formula we can deduce that the higher the transition frequency of a transistor the lower the switching time.

Also, if IB1 is high HFE IB1 is very high and tr tends towards zero.

Therefore, a high gain transistor has a smaller rise time than a lower gain transistor for the same family of products.

C-2. Turn-off time

C-2.1. STORAGE TIME

$ts = \tau s\ Ln \frac{IB1 - IB2}{Ic\ HFE - IB2}$ τ_S is defined as the constant storage time of a transistor. It varies proportionally in the same sense with the lifetime of minority carriers, and in inversely the transition frequency.

We can see that if we diminish IB1 to a minimum and if we increase IB2 we diminish ts. Also, ts is independent of Wc, depth of collector zone N-.

C-2.2. FALLTIME FOR Ic CURRENT

$$tf = HFE \left(\frac{1}{\omega T} + 1{,}7RC_{TE}\right) Ln \frac{Ic - HFE\ IB2}{0{,}1Ic - HFE\ IB2}$$

From this equation, thus turn-off times which are high when HFE is high (for the same group of products). Also, tf decreases when Ic/IB2 decreases, and is independent of IB1.

We also have: $tf = \tau\gamma\ Ln \left[\left(k + \frac{Ic}{IB2}\right)\left(\frac{Wc^2}{L}\right)\right]$

Which implies that tf is strongly dependant on Wc (depth of collector region N).

L is the length of diffusion of elections, $L^2 = \tau\gamma Dn$ in collector region N-.

$\tau\gamma$ = electron life time

Dn = electron diffusion constant

D) Ideal base control

To accelerate turn-on and reducing losses, there must be, as we have seen in the preceding chapters, a considerable IB1 peak current. Generally, Ib1 peak ≅3 Ib1 nominal gives good results. It is also important to have a generator which gives a rapid dIb/dt. If we now consider the voltage fall time we can also see that an Ib, current peak is needed.

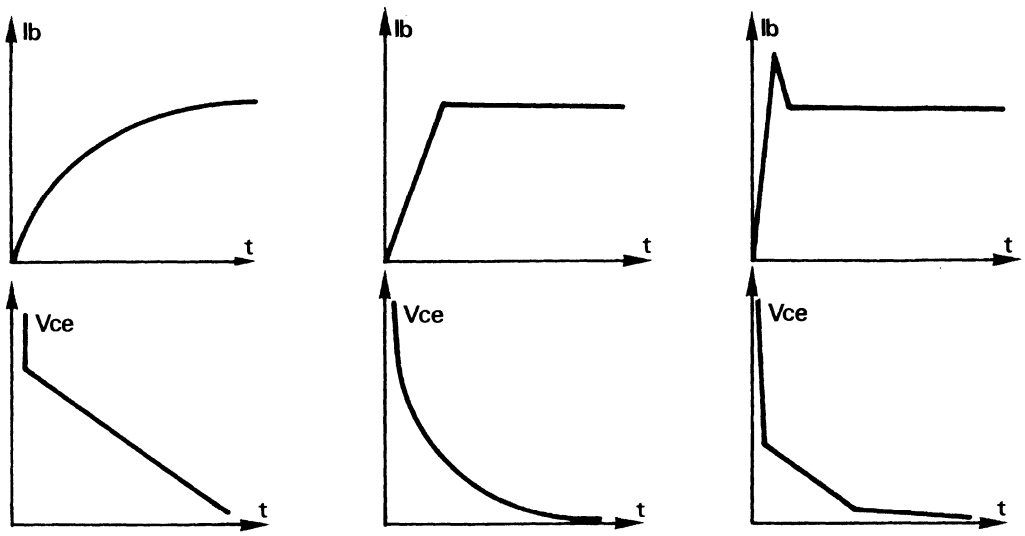


Figure 3-15 - Various voltage fall times versus, Ib_1 peak

Losses at turn-off are due, at least 50% to the descent in voltage. It is therefore doubly important to have a peak Ib1.

To accelerate turn-off, and thus permit increased operating freqency it is essential to:

– Limit the number of minority carriers stored in the collector just before turn-off. A nominal Ib1 as small as possible is essential.

– Extract as quickly as possible the carriers stored in the collector and base this a large value of Ib2. However, it is advisable to limit dIb2/dt in order to minimize tailing from rest charges.

– The dIb2/dt descent can be adjusted with the aid of a small inductance which also products a slight avalanche on the emitter base junction during turn off. For classical high voltage transistors dIb2/dt is placed below 5A/μs.

– The optimum Ib2 value versus Ic current for a low power transistor is roughly Ic/2.

We can now give the general concept of control oscillograms.

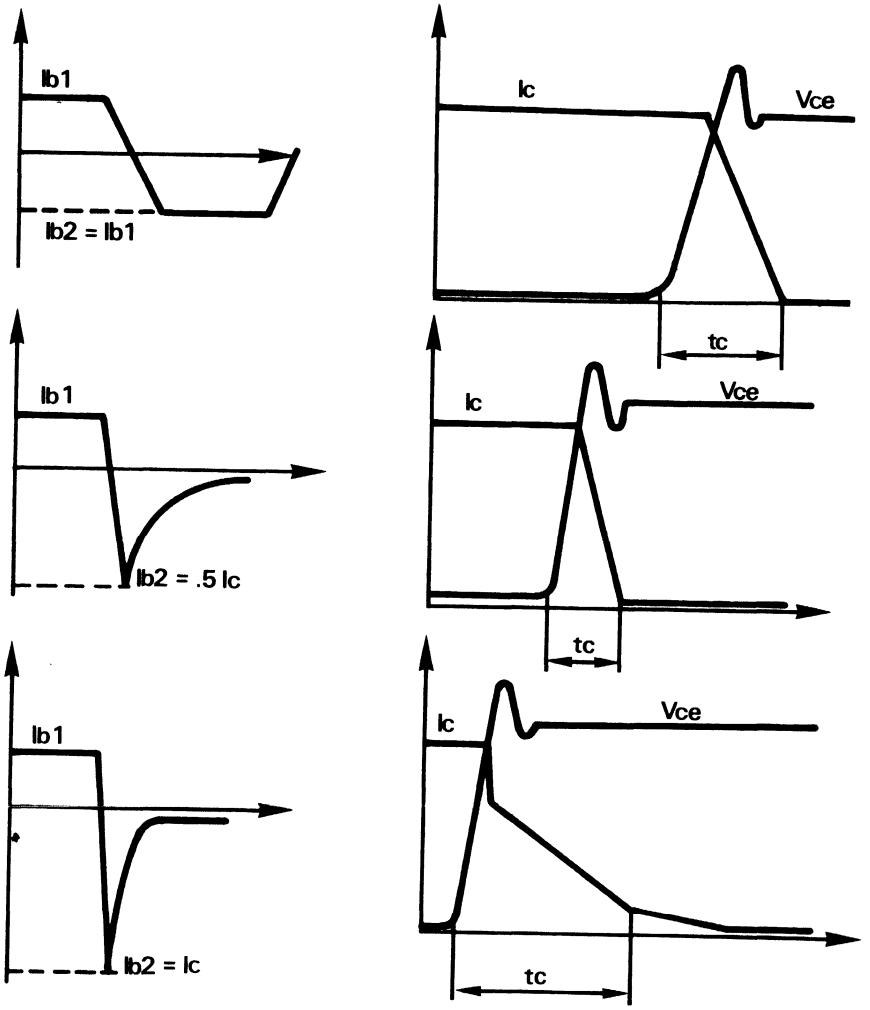


Figure 3-16 — Varius turn off behaviour versus Ib 2

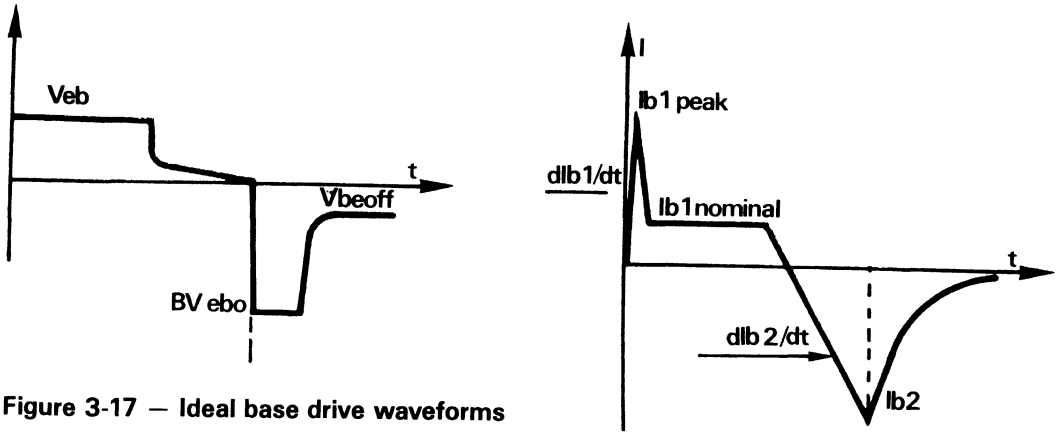


Figure 3-17 — Ideal base drive waveforms

D-1. Emitter-base junction avalanche

When the emitter-base junction is avalanched the current fall time is greatly speeded up. Emitter-base avalanche is most widely used with very high voltage power transistors, such as TV horizontal deflection output devices.

The question of long-term reliability may be raised. Since emitter-base avalanche takes place on the surface, well away from the active zone of the power transistor, it may be considered and entirely safe biasing technique.

Al Pshaenish (3) has shown that reliability is not affected by emitter-base avalanche. The gain at low level of Ic simply reduces slightly with time as shown in Figure 3-18.

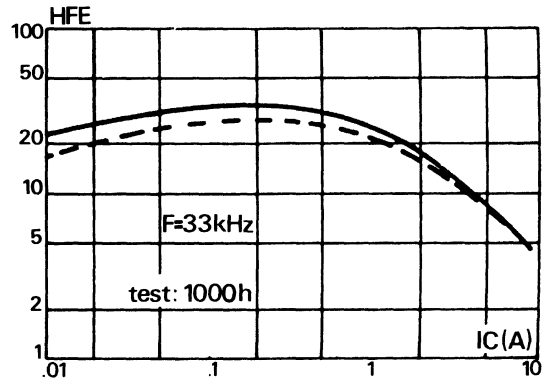


Figure 3-18 — Current gain versus BVebo

D-2. Presence of constant negative bias at turn-off

We have seen that off bias increases delay time. However, an increase in delay time is a small tradeoff compared to the benefits that can be provided. In particular, off bias may be necessary to prevent unwarted turn-on when the transistor is subjected to large values of dV/dt. In these situations, rising collector voltage is coupled to the base through the collector base capacitance. A negative base voltage will absorb this current, which otherwise can become gain multiplied and turn the transistor on.

Equally important, parasitic induction on the base lead can cause a forward base voltage to be developed. Where large energy gradients are produced, this forward voltage can exceed the transistors turn-on threshold voltage, causing unwanted turn on. For both of these reasons it is advisable to hold the transistor off with a negative bias, and keep drive loop impedance as low as possible.

E) Influence of various parameters on switch times

E-1. Influence of load current Ic

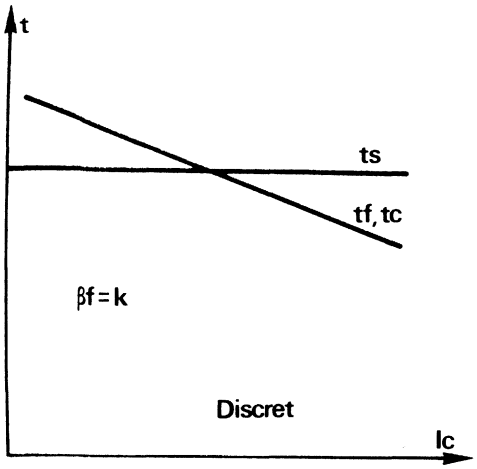


Figure 3-19 — Bipolar discrete transistor

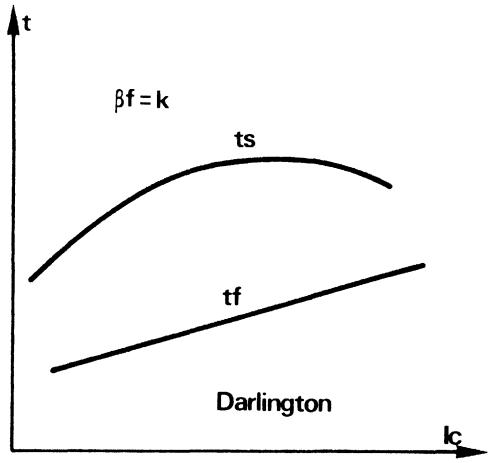


Figure 3-20 — Bipolar Darlington

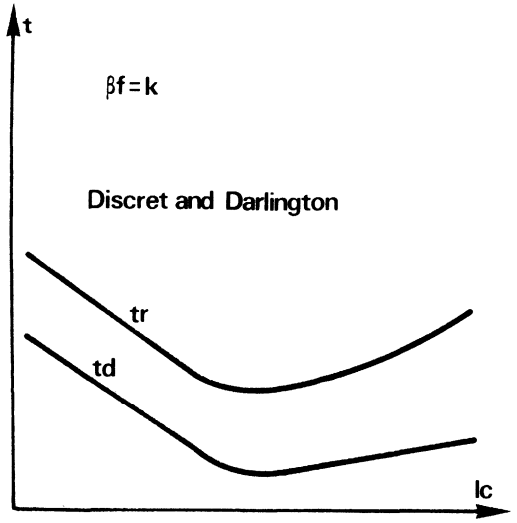


Figure 3-21 — Turn on times

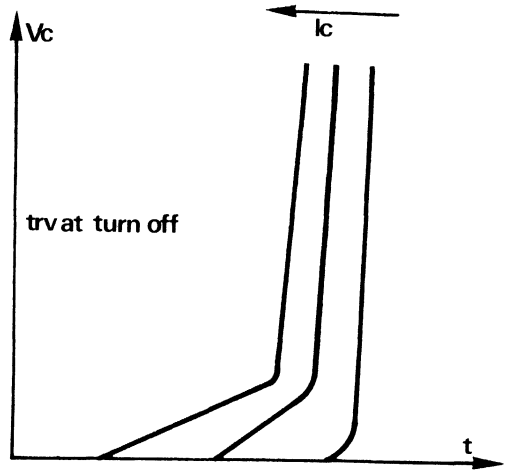


Figure 3-22 — Voltage rise times at turn off

E-2. Influence of forced gain βF

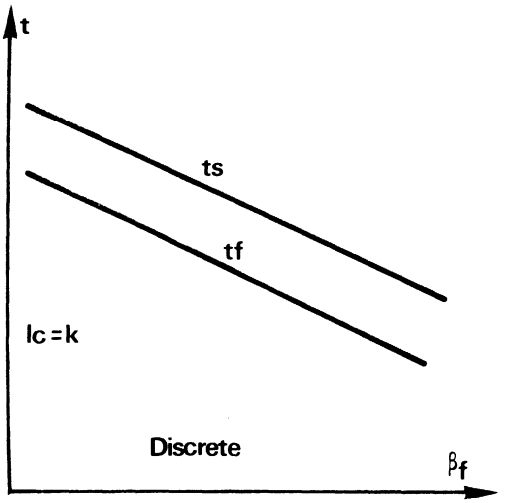


Figure 3-23 — Bipolar discrete transistor

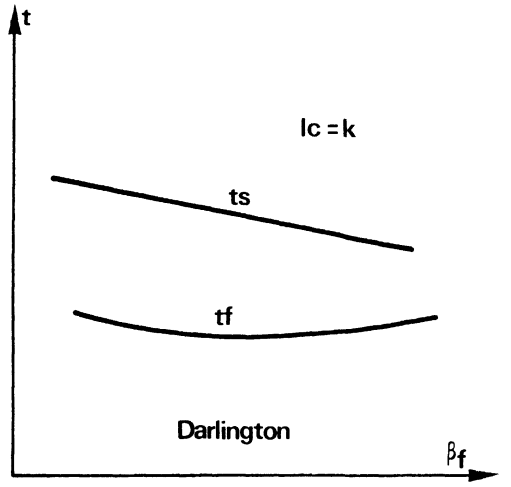


Figure 3-24 — Bipolar Darlington

E-3. Influence of Ib2 extraction current

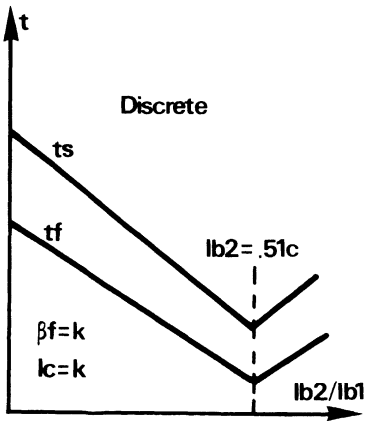


Figure 3-25 — Bipolar discrete transistor

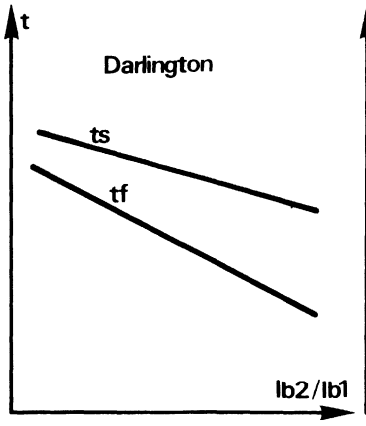


Figure 3-26 — Bipolar Darlington

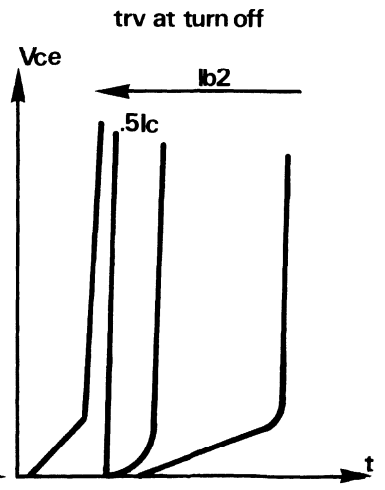


Figure 3-27 — Voltage rise time at turn off

E-4. Temperature influence

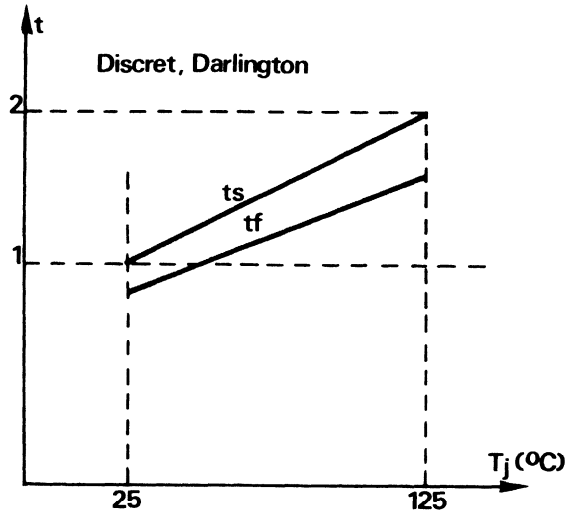


Figure 3-28 — Turn off times versus Tj

F) Current tailing

A current tail is always the sign of working in a dangerous zone. It is also highly wasteful. Attempts should be made to eliminate tailing whenever it occurs. It is useful, to understand the causes, as several physical phenomena may induce "current tails".

As we have just observed in chapter B-2.3., current tails are most commonly due to a too-rapid extraction of carriers from the base, leaving holes which must recombine in the N- collector zone.

For high voltage power transistors when the emitter base voltage applied on turn off is insufficient, tailing can be produced. It is explained as follows.

The base becomes resistive at the end of current fall time due to disappearance of excess and injection carriers (Qb).

If the extraction voltage is not sufficiently high to compensate for the drop in this resistance, there is a risk that the transistor will be still in conduction at the center of the emitter finger although it is turned off at the sides. This conduction shows up as tailing. It not only slows switching, but puts a lot of stress in a very small area, possibly affecting reliability.

There is another phenomenon which is of interest:dV/dt currents flowing into the base through the collector base capacitance can also cause tailing. As the transistor turn off, a rapid voltage rise can generate Cob coupled base current that turns the center most portion of the emitter finger on. This turning on of a portion of the structure is frequently observed as a current tail.

We will see later that base control through an RC network can bring about a non uniform current fall due to poor adaptation of the power transistor circuit.

Finally, a current tail phenomenon not directly connected to base control occurs when the product is close to its RBSOA limit. In fact, at this moment the appearance of hot spots and plasmas creates load current jumps and jettery "current tails" (Figure 3-29).

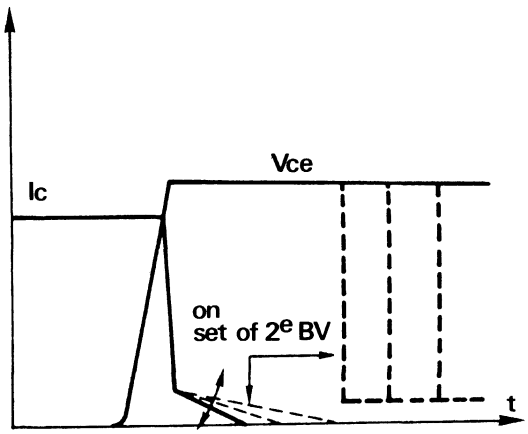


Figure 3-29 — Onset of 2nd BV

G) Anti saturation network — Baker clamp

The storage and fall times are mostly increased by hole storage in the N- collector region. We have seen in chapter B-2. that minimizing excess hole storage in this region can appreciably improve performance. A simple means of doing this is the Baker clamp.

G-1. Advantage

Figure 3-30 — Baker clamps

If we had 2 diodes, as shown in Figure 3-30a, it can be seen that "on" voltage is contrained approximately to 1 volt. At this voltage, hard saturation, and therefore, excess hole storage are avoided. If a second series base diode is added, hole storage is reduced even further. Figure 3-30b.

Another advantage of this circuit is that is avoids gross overdrive at low values of load current. The Baker clamp in effect provides a proportional base control. This is important not only for switching time, but also for RBSOA. When highly overdriven at light loads, power transistors can become quite fragile.

The circuits shown thus far have the major disadvantage of not allowing conduction of turn-off base current. Fortunately, an additional diode or a "totem pole" connection easily solve this problem. Examples are shown in Figure 3-31.

An important consideration is diode selection. The high voltage diode D2 should have a low reverse recovery time. An ultrafast recovery type such as the MUR1100 is ideal for this application. Similarly, low voltage ultrafast recovery types such as MUR105 or MUR405 are good choices for the series base diodes.

Figure 3-31– Various Baker Clamp

G-2. Results

The Baker clamp predictably improves storage times: the relative improvement is illustrated in Figure 3-32.

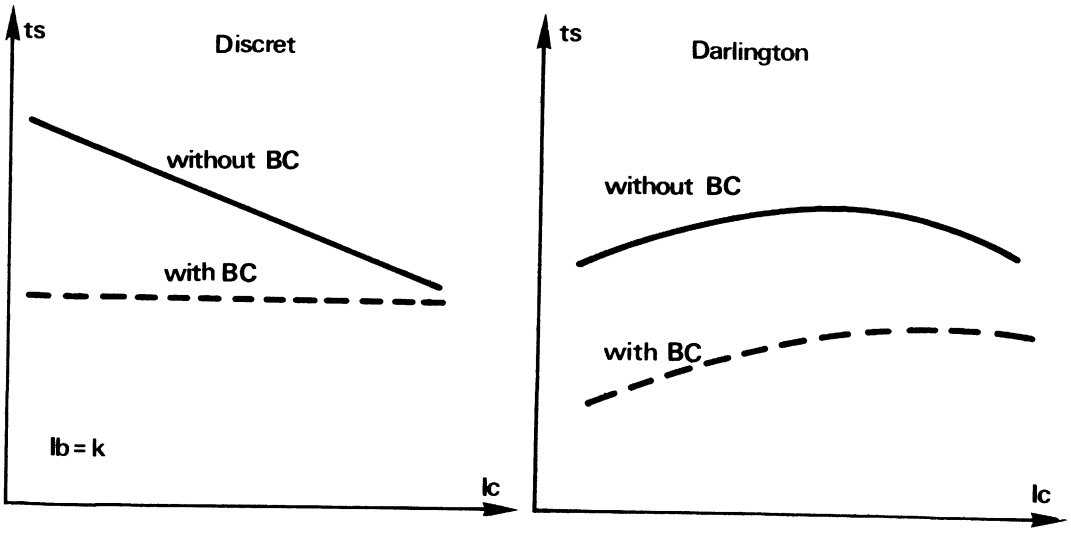


Figure 3-32 — Storage time versus Baker Clamp

G-3. Disadvantages

The prime disadvantage is the increase in conduction state losses. There therefore a compromise between improved switching and on state losses.

If the switch receives an accidental overload, an overvoltage may be created at the terminals of the product which is greater because of the trr of the D2 diode.

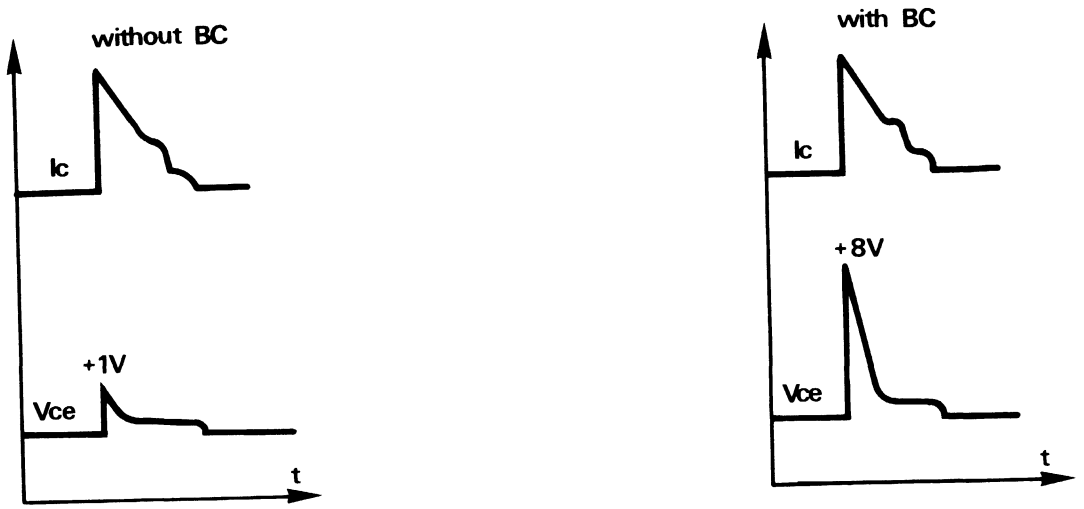


Figure 3-33 — Accidental Vce due to Baker Clamp

Due to the diodes a local oscillation is often produced up, to 4 or 5 MHz. To avoid this a high voltage but "soft recovery" diode is necessary.

Figure 3-34 — Recovery times of various diode types

If oscillations persist, ferrit beads may be used on transistor connections.

H) Examples of base control

H-1. With 2 voltage sources

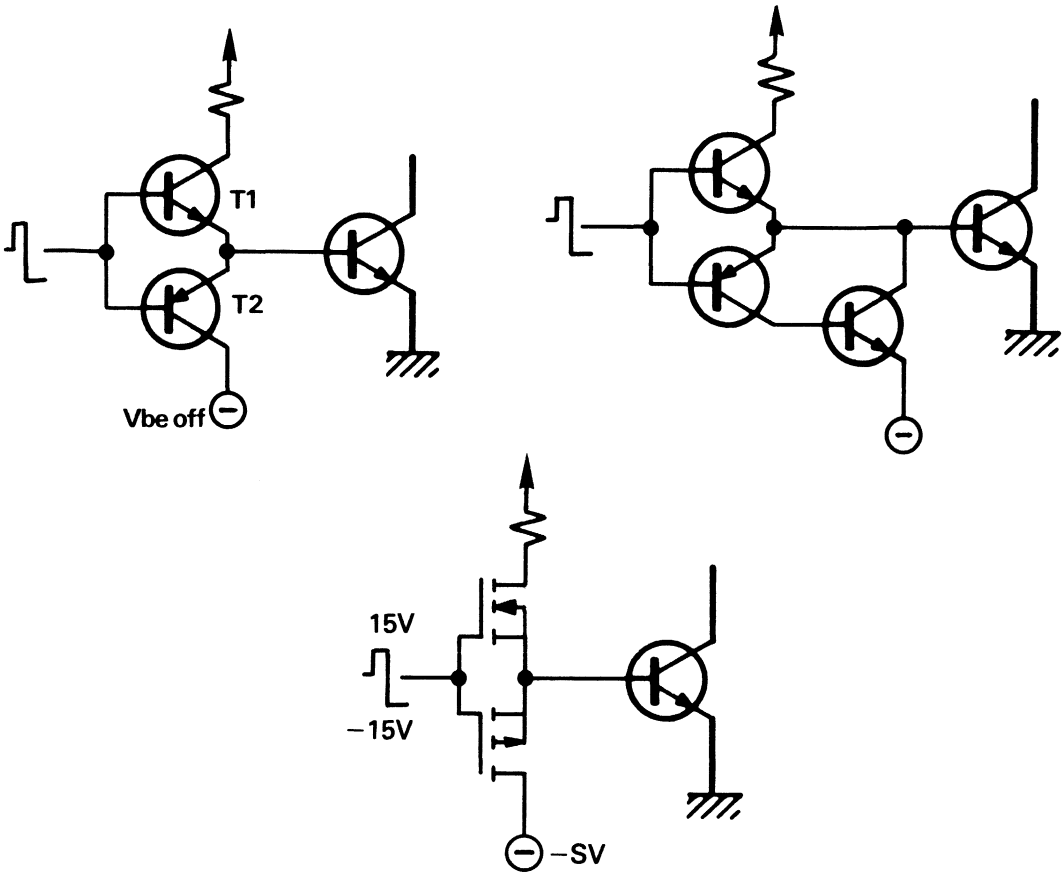
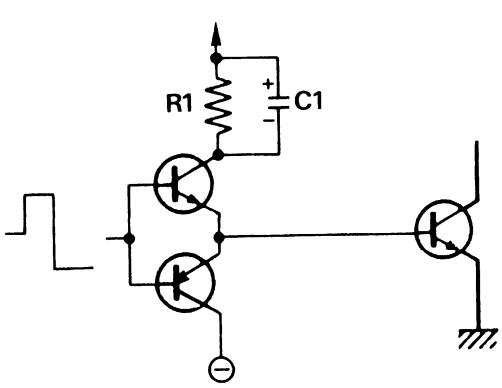


Figure 3-35 — Simple base drives

Ib(A)	T1	T2	Case
<5	BD785 MTP5N06	BD786	Case 77
<8	MJE15028 MTP10N06	MJE15029 MTP8P10	TO220
<12	BUS36 MTP15N06	BD786 BUS36 MTP15P10	TO220



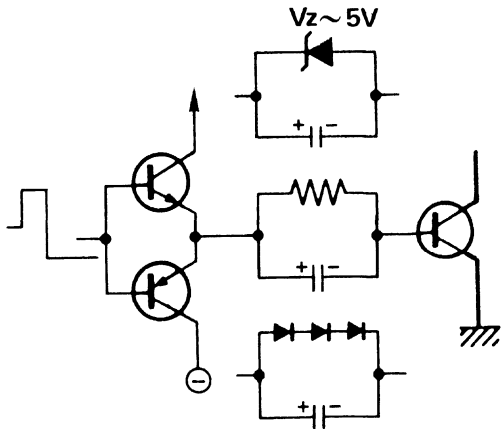


Figure 3-36 – With Ib1 overshoot

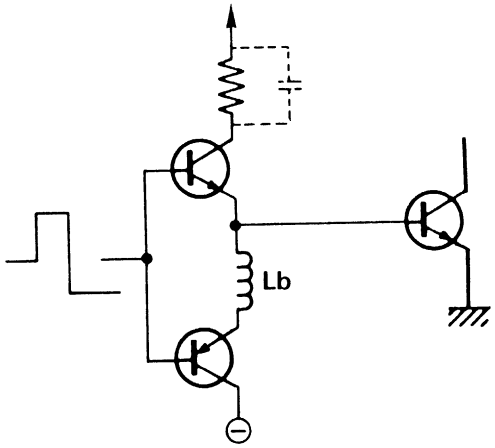


Figure 3-37 – With controlled dIb2/dt

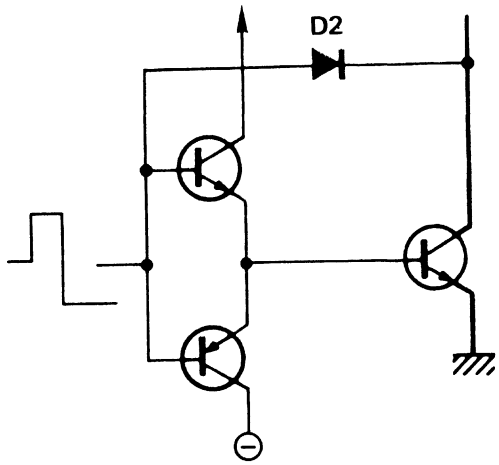
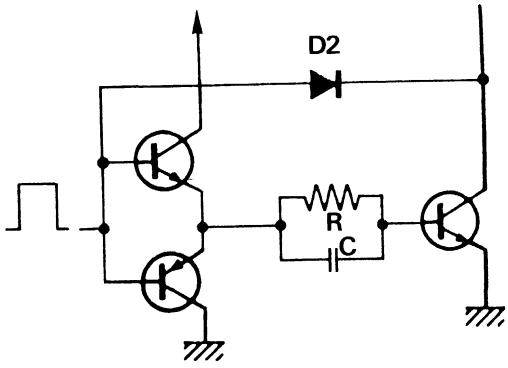


Figure 3-38 – With controlled Vce sat

H-2. With a single voltage source



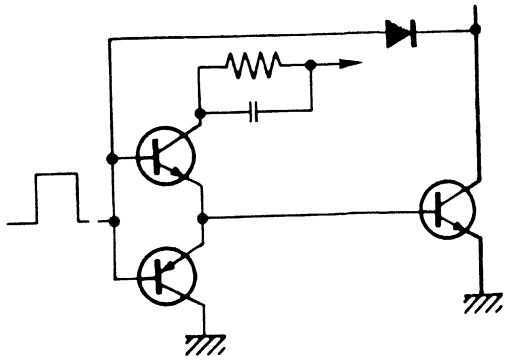


Figure 3-39 – PNP/NPN

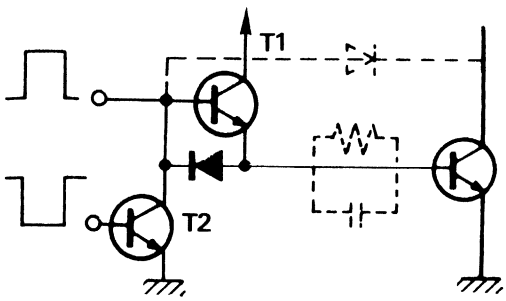


Figure 3-40 – NPN/NPN

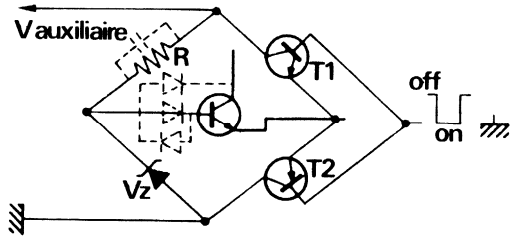


Figure 3-41 – Bridge control

H-3. Control by transformer

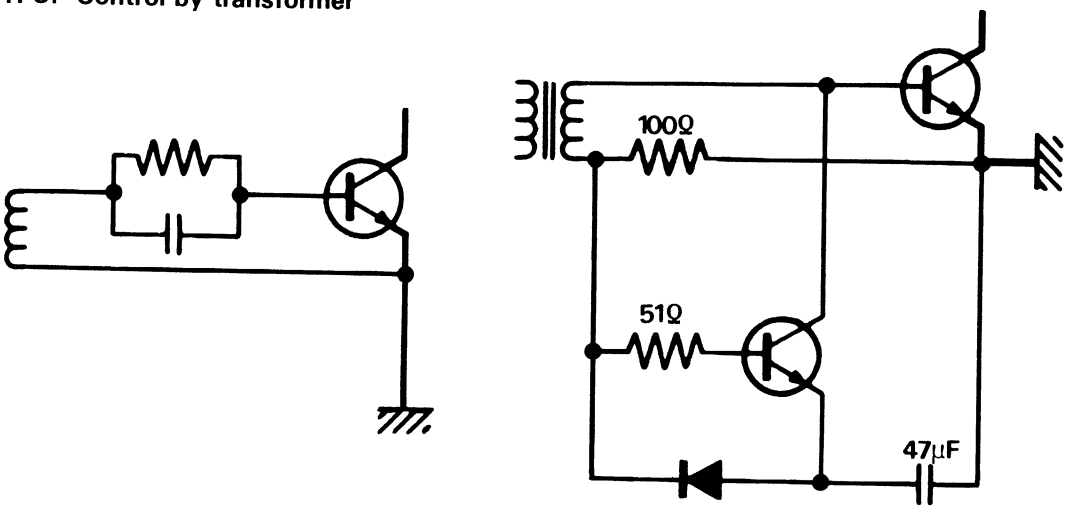


Figure 3-42 – Transformer base drives

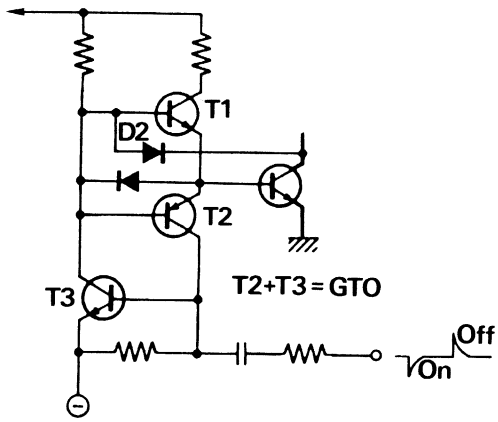


Figure 3-43 – Pulse control: GTO style

H-4. RC network control case

We saw at the beginning of this chapter that good results are achieved in terms of base drive with a circuit consisting of a parallel RC network. The problem is in the choice of components.

Resistance is first selected to give the desired off voltage of say 5 V for soft control or 10 V if an emitter-base avalanche is required.

$$\text{Thus: } R = \frac{Vsupply - (Vsat + Vbesat)}{Ib1}$$

The choice of capacitance now remains.

For this we look again at the representation according to the Ebers-Molls model.

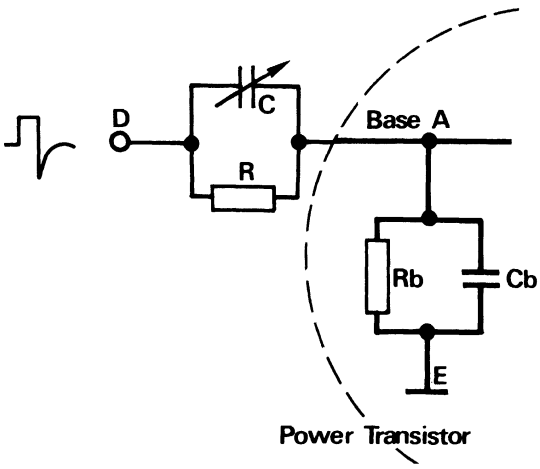


Figure 3-44 — Ebers Moll model

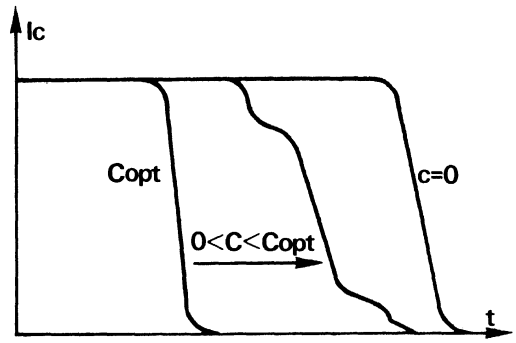


Figure 3-45 — Turn off Ic vercus C

For this type of circuit where 2 RC networks are mounted in series, if a voltage variation is required at point A identical to that of point D, RC ≅ Rb Cb is needed. For this if we look at the shape of current fall when C is varied, we obtain Figure 3-45.

For high voltage power transistors Rb Cb ≅ 5 microseconds.

If R = 5Ω, C = 1 μF is chosen, we have the following example, using a Motorola BUT16 high voltage darlington (1400V): Figure 3-46.

H-5. Proportional base drive

We have seen that with the Baker clamp we have a base control proportional to load current thus avoiding over saturation of the power transistor in cases of variable load the result is higher reliability and faster switching times.

One may also envisage a turn-off base control proportional to collector current: Ib2 ≅ kIc, Figure 3-47.

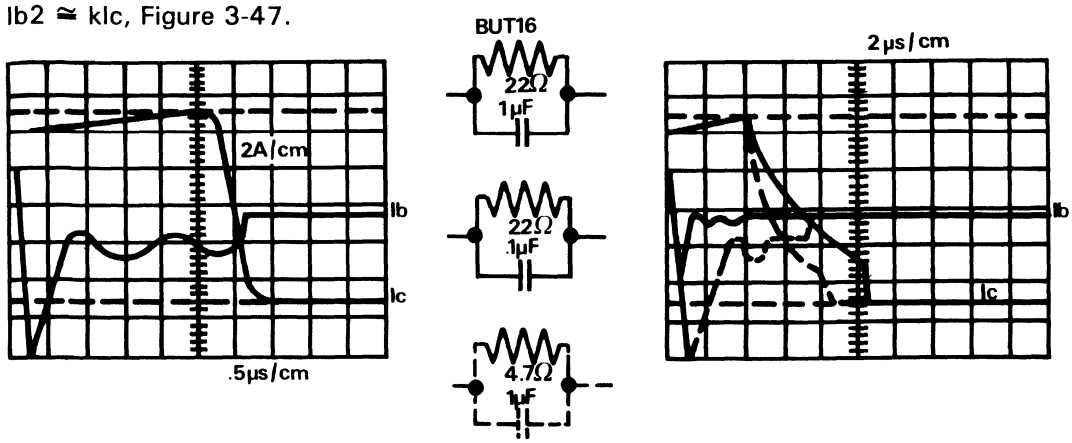


Figure 3-46 – tf versus RC

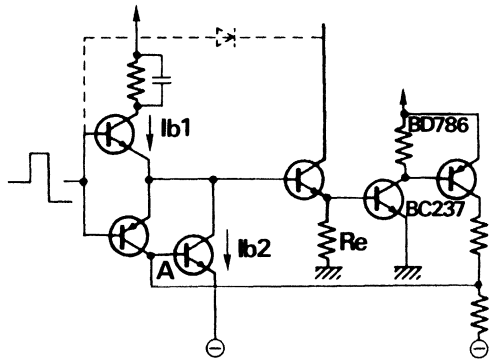


Figure 3-47 — Turn off proportional base drive

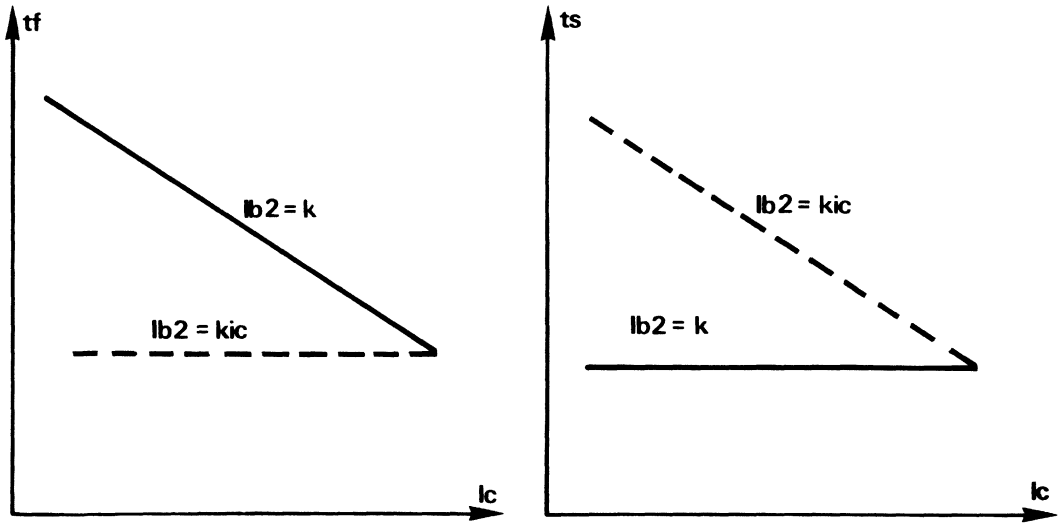


Figure 3-48 — Storage time versus Ib2

By looking at Re, one has an indication of load current Ic which is needed to turn-on the limiting circuitry. Results typical of this arrangement are shown in Figure 3-48.

One can equally produce proportional base control both for conduction and turn off. This is generally produced with the aid of a transformer which is coupled to the collector for current, $Ib1 = k_1 Ic$ $Ib2 = k_2 Ic$. According to transformer laws $k1 = N1/N2$, $k2 = N1/N3$.

See Figure 3-49, for three classical possibilities:

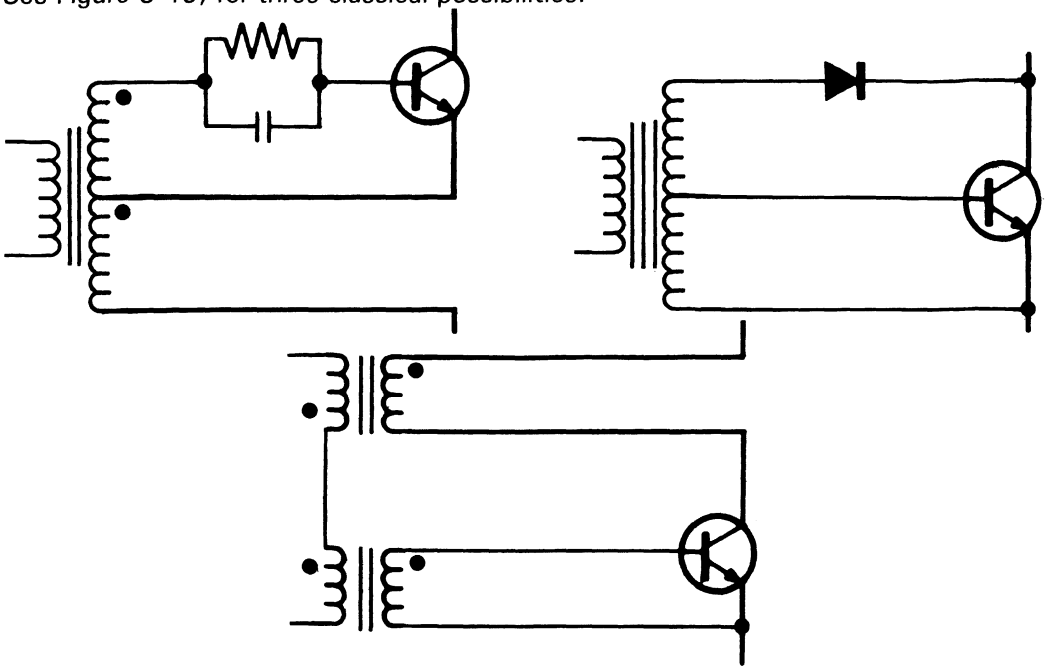


Figure 3-49 — Proportional base drive

H-6. Bibliography

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(3) AL PSHAENICH: The effect of emitter base avalanching on high voltage power switching transistors.
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2. Protection

A) Introduction

The problem of protection for semiconductor power switches (bipolar – MOS – SCR) is fairly difficult, as these products have very limited longterm overload capabilities.

Thus classical means of protection such as fuses thermistances cannot be used. Overload possibilities are first be divided into 2 categories:

- overvoltages
- overcurrents

B) Protection against overvoltages

We have seen in the chapter dealing with safe operating areas that semiconductors cannot withstand overvoltages above breakdown voltages. In an overvoltage condition, destruction is approximately instantaneous (less than 100 nanoseconds). Methods of overvoltage protection must therefore be very fast, and be wired in a manner which involves little delay time. Transient power-suppression zeners usually have the qualities required for good protection. They are effective for fast, very short pulses. Connection is usually between the collector-emitter terminals of the power transistor, although some applications effectively increase the power rating of the zener with a collector-base connection. Alternately, a capacitor connected between collector and emitter terminals performs the same function. This approach, however, soffers from a tendency to slow switching times. A third alternative is diode clamping with an auxillary power supply.

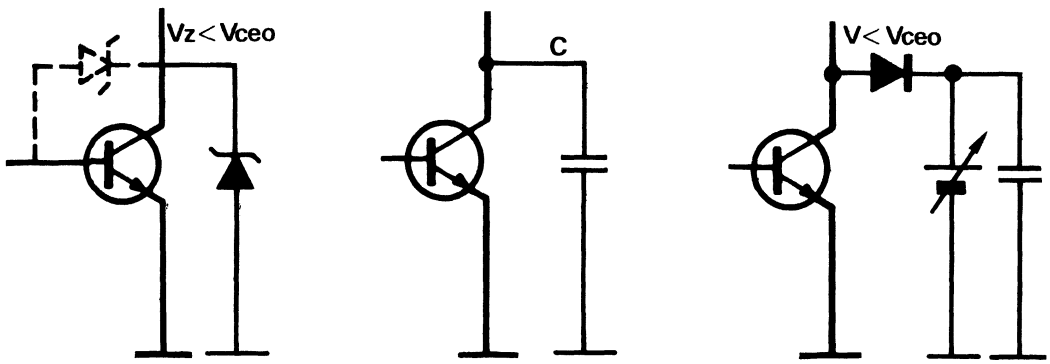


Figure 3-50 — Transient overvoltage protections

C) Protection against overcurrents

Semiconductors have a very great ability to survive temporary overcurrents, as long as these do not exceed thermal limits.

One can in fact, now look at the manufacturer's data sheets of overload curves (OLSOA – Overload Safe Operating Area) which a permit currents greater than 5 times the nominal current (Figure 3-51).

The real problem is the switch off point. Since the current is high, dI/dt is also high and small amounts of parasitic inductance gives us a large di/dt generated voltage. We have thus a far more dangerous overvoltage defect.

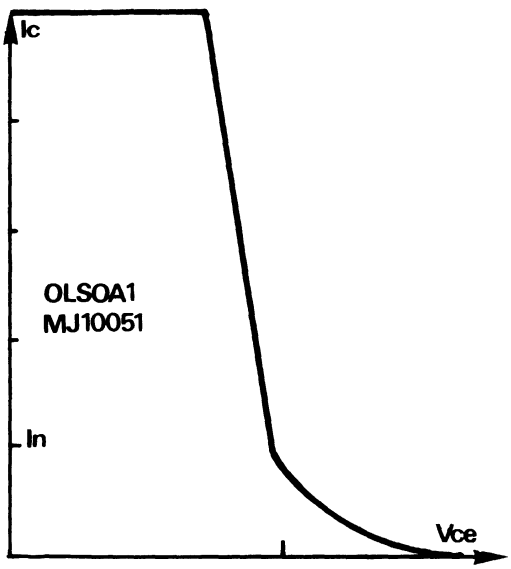


Figure 3-51 – OLSOA

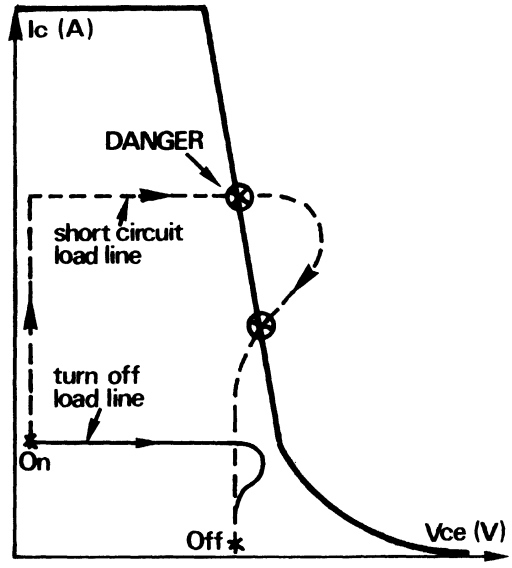


Figure 3-52 – Short circuit load line

A protection system for overcurrent should therefore be rapid. The maximum current reached is equal to $Imax = I\ nominal \left(1 + \frac{R}{L} \Delta t\right)$

Since inductance is small, large currents can be obtained. Δt consists of not only detection delay but also the reaction time of the system and the storage time of the switch. Following this, V supply + ΔV are checked to determine if safe voltage limits are exceeded. If peak voltage exceeds acceptable limits, some form of load line shaping is required.

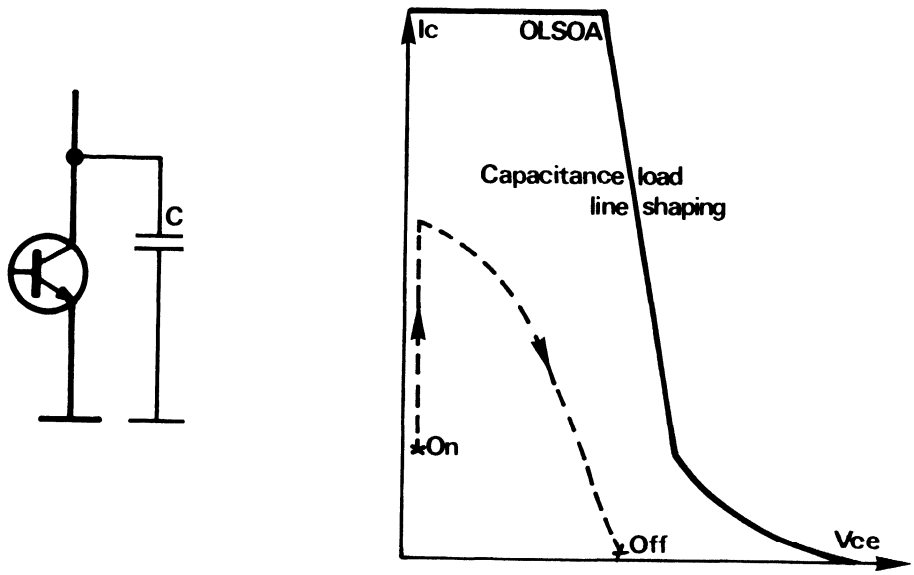


Figure 3-53 – Effect of a capacity on load line at turn off

D) Protection techniques

Before looking at different protection techniques, possible phenomena are considered:

Hard short circuit, dI/dt limited by wiring and transistor

Switch-on of system

Temporary, very short-lived overload.

Detection systems should be capable of discriminating between these different phenomena and of reacting accordingly:

- switching off system, manual reoperation only,

  temporary disabling of the detection system for a period sufficiently long, to avoid starting transient oscillations, but, sufficiently short, to cut-off in case of switching on into short-circuit,

- automatic limitation of transient energy until the fault removed.

Protection techniques may be divided into 3 general categories:

- Measurement of current by resistance voltage drop
- Measurement of current by current transformer
- Measurement of transistor desaturation

We shall see through several examples advantages and disavantages of each type of protection.

D-1. Detection by resistance

Load current flowing through R1 is threshold detected and compared with a voltage reference. A comparator is triggered which will either block the transistor temporarily or fire thyristor for shutdown, if the threshold is exceeded. The comparator is rendered inoperant during the switching on of the system.

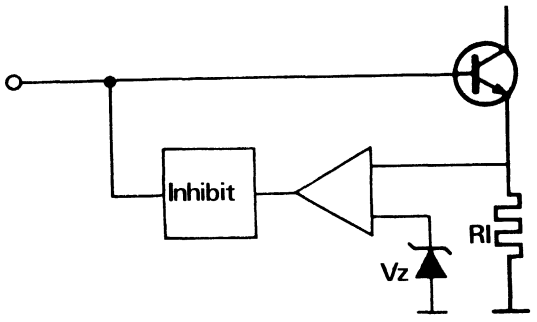


Figure 3-54 – Basic diagram

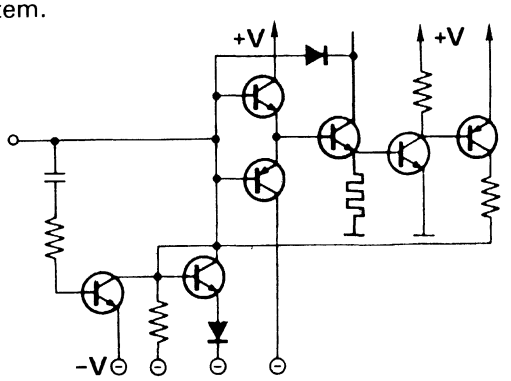


Figure 3-55 – Tempory inhibit – Tempory shutdown of switching on transistors

This system has the advantage of being simple and inexpensive but it consumes energy thus reducing overall efficiency.

D-2. Detection by transformer

The guiding principle is identical, only the detection of fault changes.

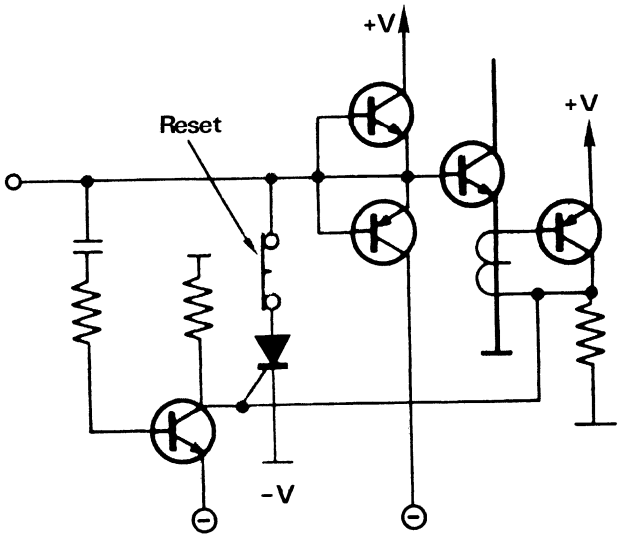


Figure 3-56 – Turn-on disabling of protective system

This system has the advantage of not consuming energy but may be limited in very high dI/dt situations.

D-3. Measure of transistor desaturation

The detection system here is completely different. The rise in voltage at transistor terminals is used as the sensing mechanism load current increases with constant Ib, an abrupt increase in Vce is detected.

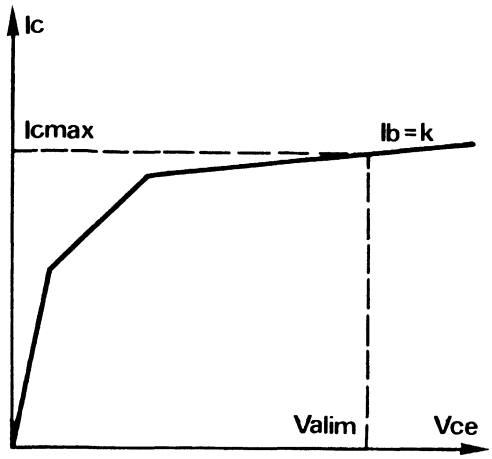


Figure 3-57 – Maximum current in short circuit

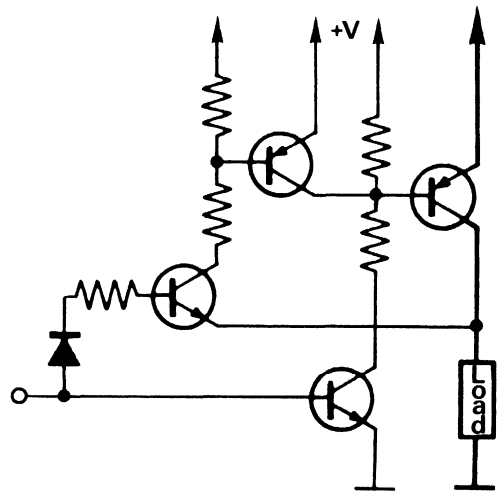


Figure 3-58 – Detection of VCEsat

The value of the short circuit current being equal to Isc = HFE Ib. This system has the advantage of consuming no energy and of not being limited by dI/dt. The only problem is the phase-delay which usually occurs between the rise in load current and the collector emitter voltage. This delay is usually about 4 to 6 microseconds, and is sufficient to attain large values of short-circuit current before turning off.

To diminish this phase-delay, the rise in emitter-base voltage may be used when Ic increases.

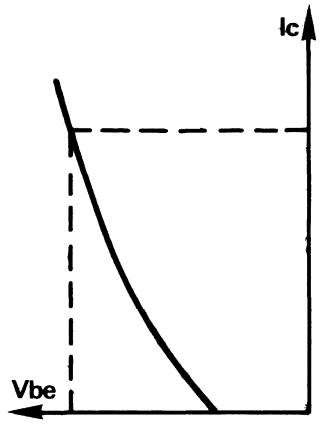


Figure 3-59 – IC = f(Vbe)

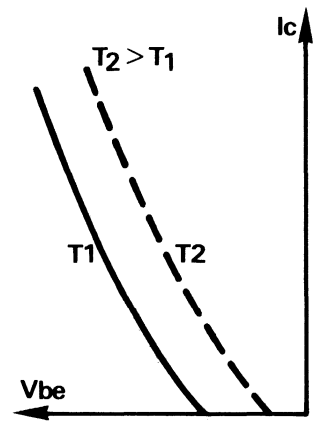


Figure 3-60 – Effect of temperature on the Vbe

This system is easy to set up on Darlingtons as Vbe is sufficiently large to be detected from outside noise. For discrete transistors it is more difficult due to lower Vbe. An added complication is that Vbe decreases when the case temperature increases, producing and inherent inaccuracy.

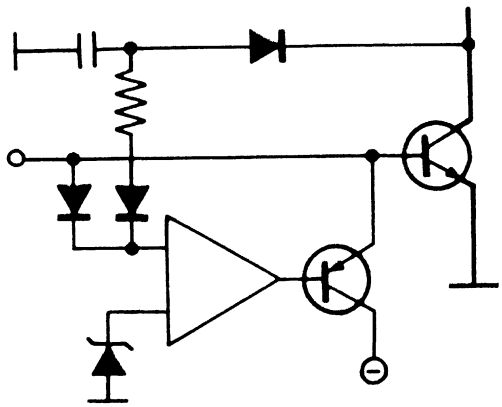


Figure 3-61 – Detection of Vce and of Vbesat

For efficient detection we could use a combination of both systems: Vce and Vbe detection together.

E) Conclusion

The overriding consideration for protection circuits is to ensure that the load line remains within acceptable limits. Centralized protection systems do not usually meet this criteria, since transient overstress in a power system can be highly localized in nature. Therefore, individual protection of power switches is usually necessary for reliable operation.

E-1. Bibliography

(1) A. BRADJER: Improved short circuit protection of power transistors and Darlington – PCI 82, Geneva.

3. Load line shaping circuits (or snubbers)

A) Switch turn-off losses with an inductive load

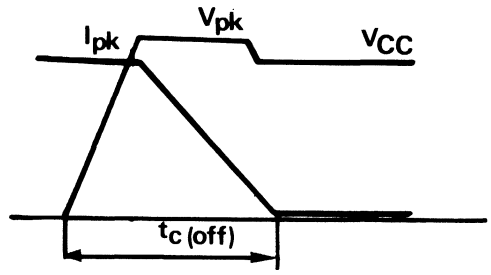


Figure 3-62 — Turn off waveform

For each pulse: turn off losses are equal to:

$E_{off} = \frac{1}{2} V_{PK} I_{PK} t_{c(off)}$ assume a linear decrease in current and no tail. In reality due to non linear rises and falls and current tails this approximation of turn off losses should be checked using piece wise integration techniques.

B) Switch turn on losses with a capacitive or free wheeling diode load

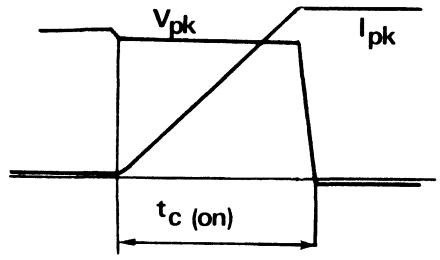


Figure 3-63 — Turn off waveform

For the same ideal conditions, one can also say that the losses in the transistor for each pulse are:

$$E_{ON} = \frac{1}{2} V_{PK} I_{PK} t_{c\ (on)}$$

C) Snubbing circuit calculations

Calculating Cs for turn off snubbing. To change from an inductive to a resistive load line. The rise in voltage at terminals of snubbing capacitor Cs or of power transistor VCE is equal to:

$$VCE = VCS = \frac{1}{CS}\int_0^t Is\,dt \qquad \boxed{VCE = \frac{1}{2}\frac{1}{CS}\frac{I_{PK}}{tf}t^2}$$

Since the capacitor current is linear in relation to time and equal to: $I_{CS} = \frac{I_{PK}}{tf}t$

If one adjusts Cs to obtain VCS = VPK at the end of tf, it can be written as:

$$\boxed{CS = \frac{I_{PK}\ tf}{2V_{PK}}}$$

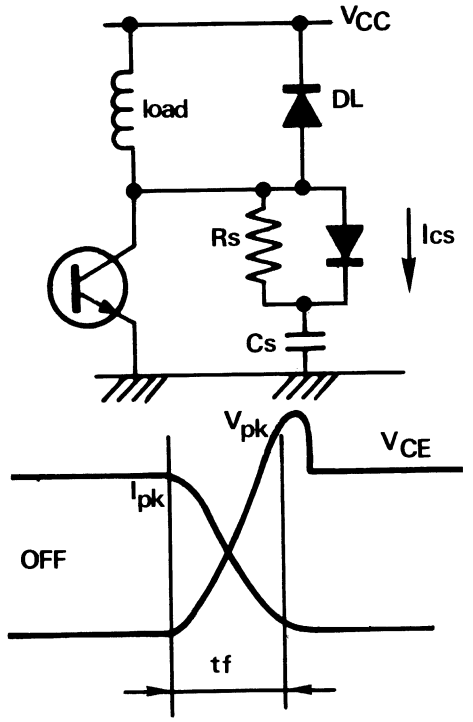
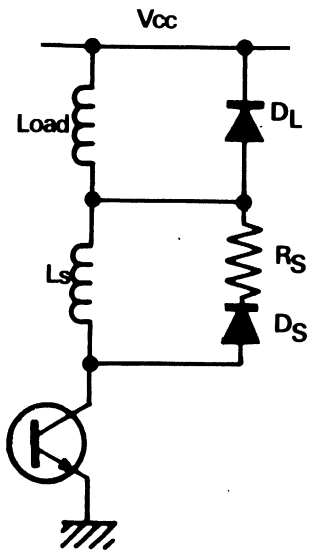


Figure 3-64 — Complete circuit

Calculating LS for turn on snubbing.



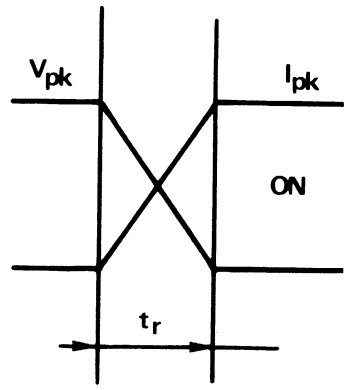


Figure 3-65 – Turn on

May also be written as: $\boxed{L_S = \frac{V_{PK}\ tr}{2\ I_{PK}}}$

for reasons of duality if I in transistor = I load at the end of tr.

D) Optimizing losses with snubbing circuits

D-1. At turn off, for each pulse $E_{off} = \int_0^{tf} I_C\ V_{CE}\ dt$

with $I_C = I_{PK}\ (1 - \frac{t}{tf})$ and $V_{CE} = V_{CB} = V_{PK}\ (\frac{t}{tf})^2$

$$W_{off} = V_{PK}\ I_{PK} \int_0^{tf} (1 - \frac{t}{tf})(\frac{t}{tf})^2\ dt \qquad \boxed{E_{off} = \frac{1}{12}\ V_{PK}\ I_{PK}\ tf}$$

D-2. At turn on, by pulse, by duality $\boxed{E_{on} = \frac{1}{12}\ V_{PK}\ I_{PK}\ tr}$

If we choose values C and L for snubbing circuits different from ideal values CS and LS, we have:

$$E_{off} = \frac{1}{12}\ V_{PK}\ PK\ \frac{CS}{C}\ tf$$

$$E_{on} = \frac{1}{12}\ V_{PK}\ PK\ \frac{LS}{L}\ tr$$

D-3. Energies stored in the snubbing network are:

$$E_C = \frac{1}{4} V_{PK}\ I_{PK}\ t_f \frac{C}{CS} \qquad E_L = \frac{1}{4} V_{PK}\ I_{PK}\ t_r \frac{L}{LS}$$

D-4. Total losses are the sum of the preceding energies:

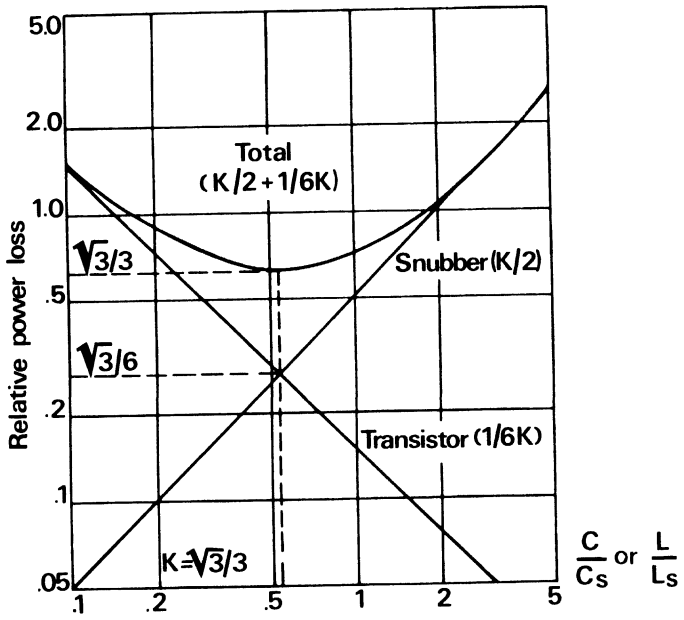
$$E_{on\ total} = \frac{V_{PK}\ I_{PK}\ t_r}{2}\left(\frac{1}{6}\frac{LS}{L} + \frac{1}{2}\frac{L}{LS}\right)$$

$$E_{off\ total} = \frac{V_{PK}\ I_{PK}\ t_f}{2}\left(\frac{1}{6}\frac{CS}{C} + \frac{1}{2}\frac{C}{CS}\right)$$

By differentiating with respect to L, one can define a minimum of losse when:

$$-\frac{1}{6}\frac{Ls}{L^2} + \frac{1}{2Ls} = 0 \quad \text{or} \quad \left(\frac{L}{LS}\right)^2 = \frac{1}{3} \quad \text{or} \quad L = \frac{LS}{\sqrt{3}} \quad \text{by duality} \quad \left(\frac{C}{CS}\right)^2 = \frac{1}{3} \quad \text{or} \quad C = \frac{CS}{\sqrt{3}}$$

see graph below :



Ratio $k = \frac{L}{L_S}$ or $\frac{C}{C_S}$

Figure 3-66 – Loss distribution

E) Practical snubbing circuits

E-1. Add Cov to limit the voltage overshoot due to parasitic inductance (LF).

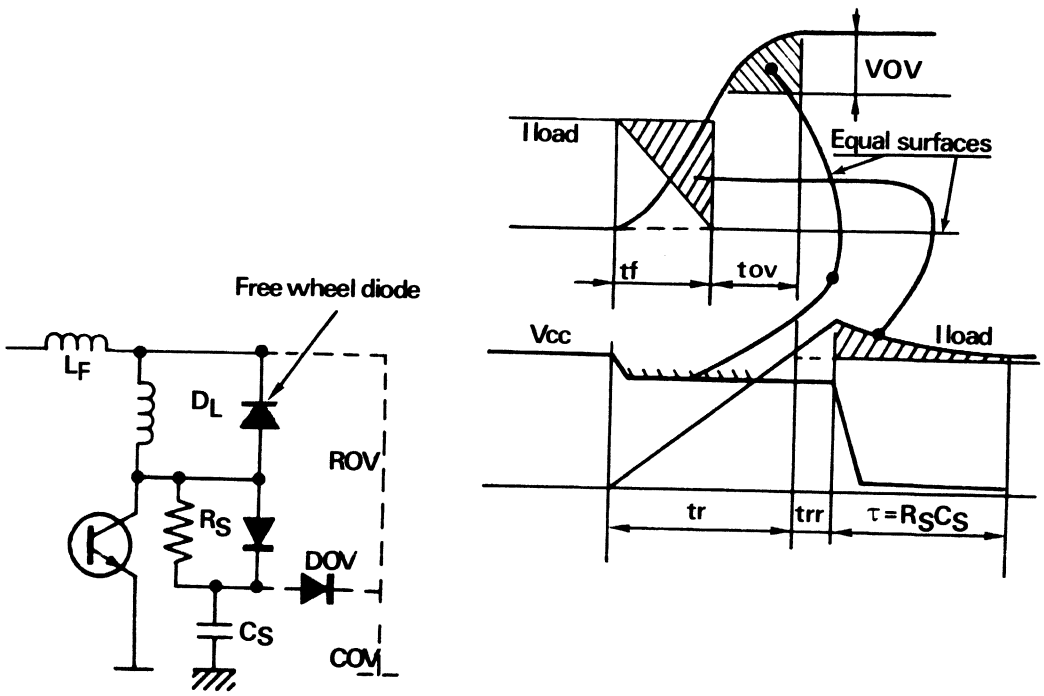


Figure 3-67 – Complete circuit

Let us suppose Irec of freewheeling diode DF. Irec = 0,3 Iload and suppose that RS is chosen such that:

$$RS = \frac{V_{CC}}{0\,3\,I_L}$$

the constant capacity discharge time is:

$$I = \frac{V_{CC}}{0.3 I_L} \frac{I_L t_f}{2 V_{CC}} = \frac{t_f}{0.6} = 1{,}67\, t_f$$

The 2 shaded areas on the current waveforms must be the same, let us suppose there is a parasitic inductance (of wiring, transformer leakage) LF such that overvoltage without snubber is: VOV1 = 0,1VCC LS = 0,1VCC tf/Iload

Where VOV1 = LS dI/dt with dI = Iload and dt = t_f with shunt snubbing circuit (capacitive) we have

$$VOV = ILoad\sqrt{\frac{L_f}{C_s}} = I_L\sqrt{\frac{0{,}1V_{CC}\,t_f}{I\text{load}} \times \frac{2V_{CC}}{I\text{load}\,t_f}} = V_{CC}\sqrt{0{,}2} = \boxed{0{,}45V_{CC}}$$

The overvoltage due to snubbing shunt with parasite inductance is higher than if the snubbing circuit did not exist.

0,45 Vcc instead of 0,1 Vcc

The two shaded areas on the voltage waveforms must be identical.

If this overvoltage cannot be allowed LF must be minimised and another COV and ROV must be added where COV ≅ 10 Cs. It is also possible to use a standard snubbing circuit such as the following:

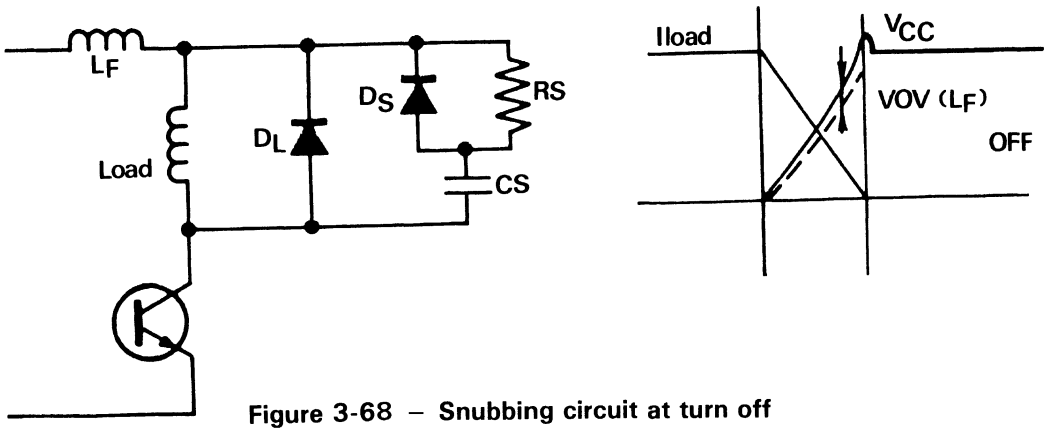


Figure 3-68 – Snubbing circuit at turn off

We do not need a COV ROV circuit for an overvoltage which is 10% of Vcc without the snubbing circuit. If C is greater than calculated CS no overvoltage protection circuit is needed.

E-2. Snubbing circuit at turn off

Consisting simply of a capacitance plus resistance.

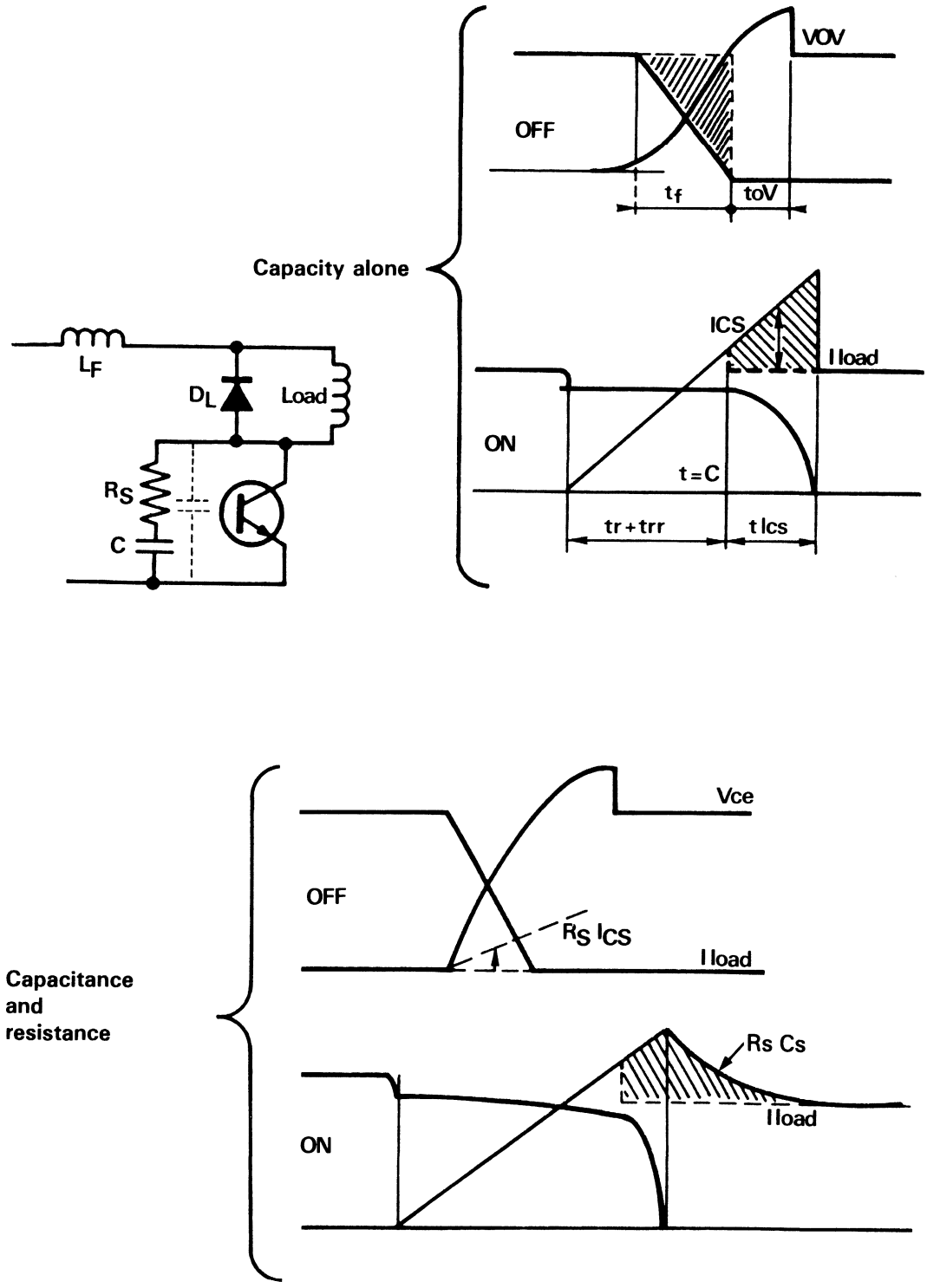


Figure 3-69 – Snubbing circuit at turn off

We have the following equations:

$I_S = Irec + \frac{I_L}{tr} t$ and $Vce = Vcc - Rs\ I_S - \frac{1}{C}\int_0^t I_S\ dt$ The additional turn on losses are:

$E_{on} = \int_o^{to} (I_S + I_L)\ Vce\ dt$ If one choose $R_S = 0{,}5\ \frac{Vcc}{Iload}$ and $C = 2Cs$

The turn off trace in the I X V plane is approximately the same as with RS = 0 and C = CS, but the OFF losses in the transistor increase by 50%.

$$Eoff = \frac{Vcc\ Iload}{24} t_f$$

One can thus construct a table of different losses according to the case chosen with Irec = 0.3I Load.

Table 3-1 – Distribution of losses due to RC turn off snubbing circuit

	C = Cs Rs = 0		C = 2 Cs RS = .5 Vcc/Iload
Off losses without snubbing	$E_{off} = \frac{1}{2}$ Vcc Iload t_f = K		
Off losses with snubbing	K/6		K/4
Off losses saving	5/6 K		3/4 K
On losses without snubbing	tr = t_f	$E_{on} = \frac{1}{2}$ Vcc Iload tr = K	
Additional turn on losses	tr = t_f	1.38 K	1.06 K
	tr = .5 t_f	1.2 K	1.072 K
ratio turn Off saving	tr = t_f	.6	.7
ADD On losses	tr = .5 t_f	.66	1.04
Additional turn On losses for Iload = 0	tr = t_f	K/2	.42 K
	tr = .5 t_f	.43 K	.3 K

We can see on this table that for tr = t_f and for the same trace in the I.V plane at turn off there is no large difference in losses between a capacitance alone and an R.C. circuit.

For tr < tf, the RC becomes clearly more favourable.

E-3. Snubbing circuit at turn on

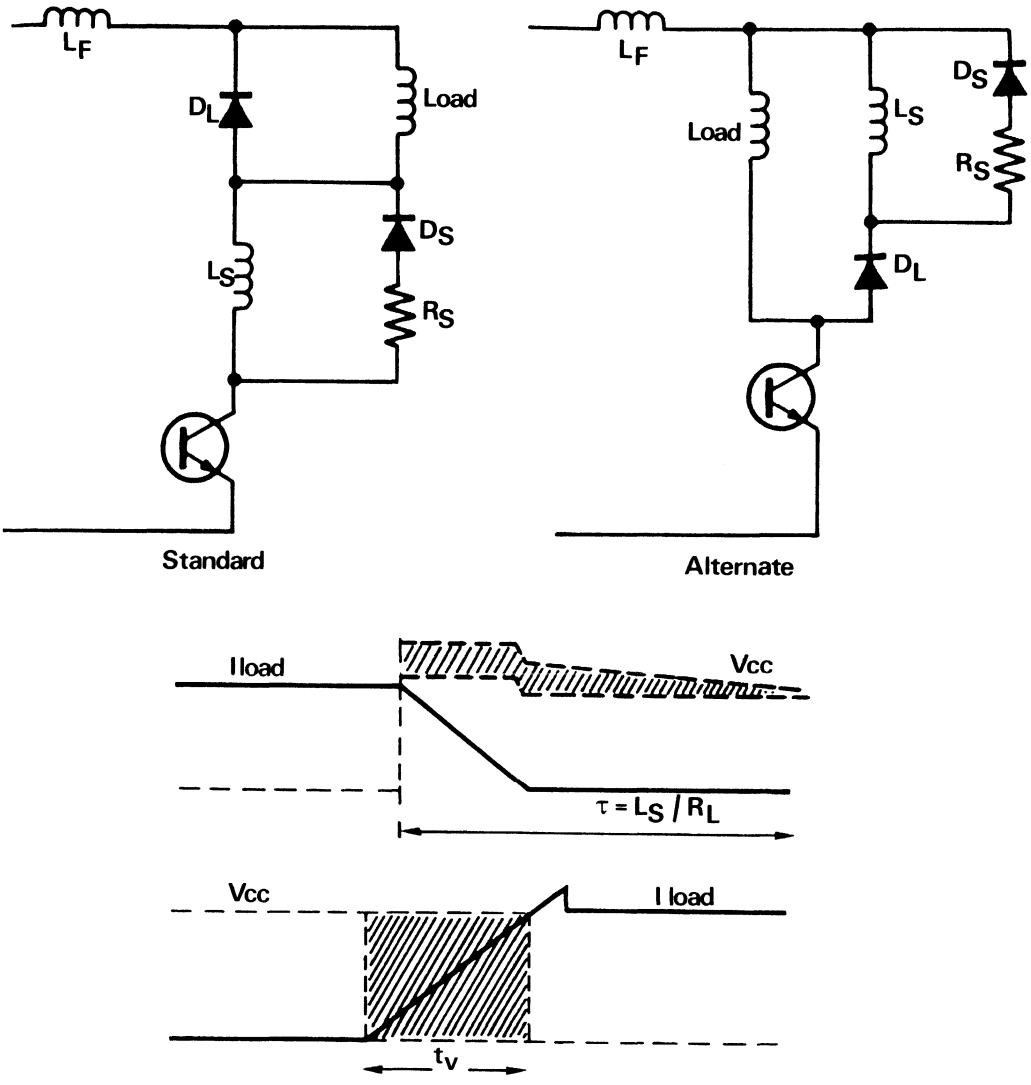


Figure 3-70 – Snubbing circuit at turn on

We see from the waveforms that the energy absorbed by the LS inductance at turn on is restored at turn off (equal shaded areas).

F) Complete snubbing for turn off and turn on

F-1. Series and shunt snubbers

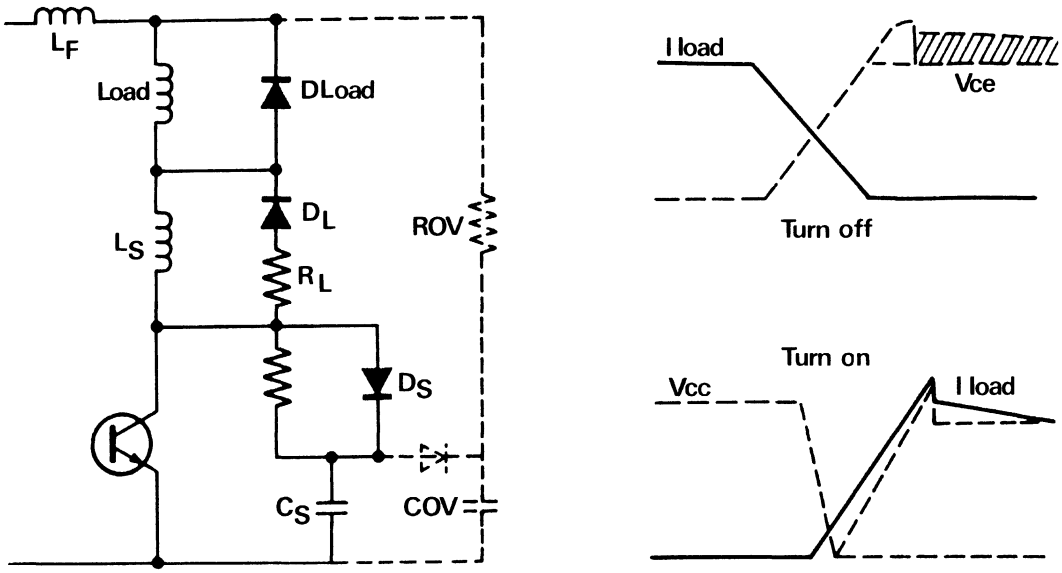


Figure 3-71 – Complete snubbing circuit

If we combine Figures 3-67 and 3-70, we obtain the circuit and waveforms of Figure 3-71. At turn on up to IC ≦ Vcc/RS the current in the LS inductance increases very slightly (dotted), the capacitor of the shunt snubber is nearly discharged during the current rise.

F-2. Common resistance snubber

We can also place snubbers as shown below:

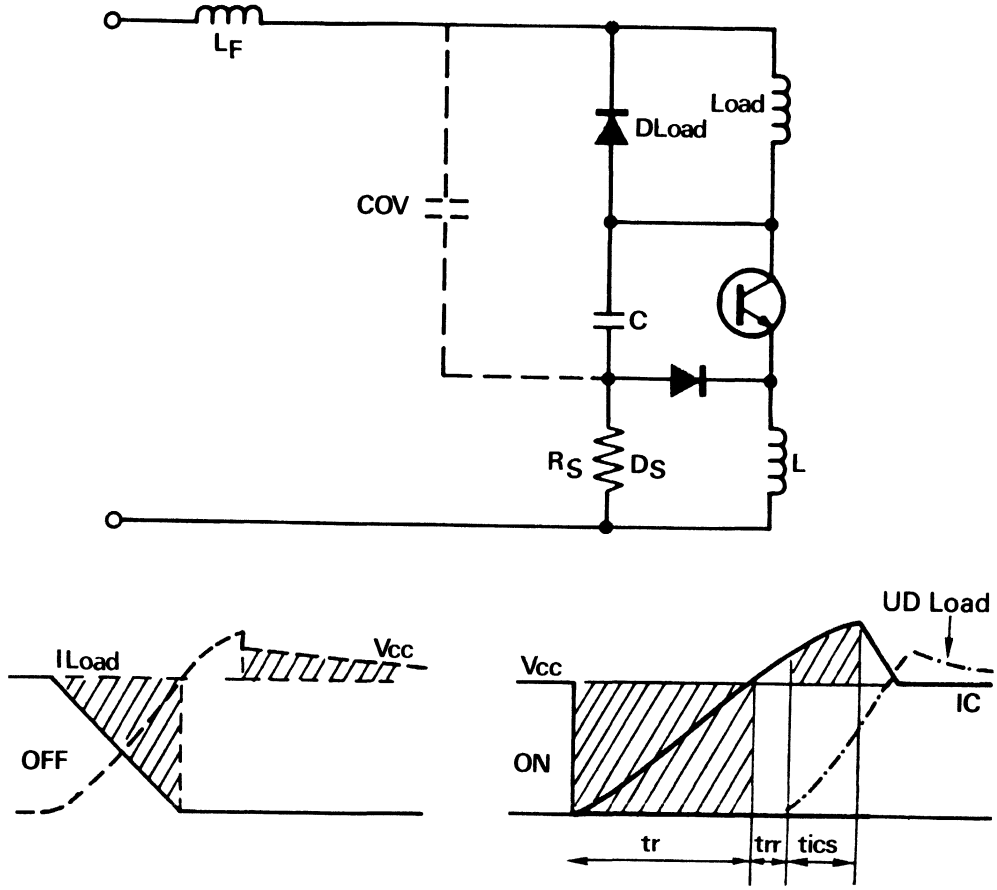


Figure 3-72 – Common resistance snubber

The waveforms are identical to those in the previous figure: at turn on after diode DL recovery time we have discharge R_S C of the capacitance and the snubbing inductance (R_S L).

The energy stored in the network is: $ES = \frac{1}{2} L\, Irr^2 + \frac{1}{2} C\, Vcc^2$ with $C = k_c CS$ and $L = k_L LS$ and

$$C_S = \frac{I_L\, t_f}{2\, Vce} \text{ and } L_S = \frac{Vcc\, tr}{2\, I_L}$$

(from equations (4) and (5) which were derived earlier) so:

$$E_S = 1/2\, L_S\, I^2 rr + 1/2\, \frac{I_L t_f}{2}\, kc\, \frac{2\, IL\, LS}{t_r\, k_L} = 1/2\, L_S \left(I^2 rr + \frac{kc}{k_L}\, \frac{t_f}{tr}\, I_L 2\right)$$

We can say that the snubbing network adds a ΔI current such as: $ES = \frac{1}{2} LS\, (Irr + \Delta I)^2$

– or also

$$Irr^2 + \frac{kc}{kL}\frac{tf}{tr} I^2L = (Irr + \Delta I)^2$$

if kc = 1 kL = 1 t_f = tr we have $\Delta I = 0{,}74\ I_L$ If KL = 3 the rest being identical $\Delta I = 0{,}35\ I_L$ but instead of increasing LS it is usually more practical to reduce C (kc<1).

One can rearrange the snubber in Figure 3-72, according to the following diagrams.

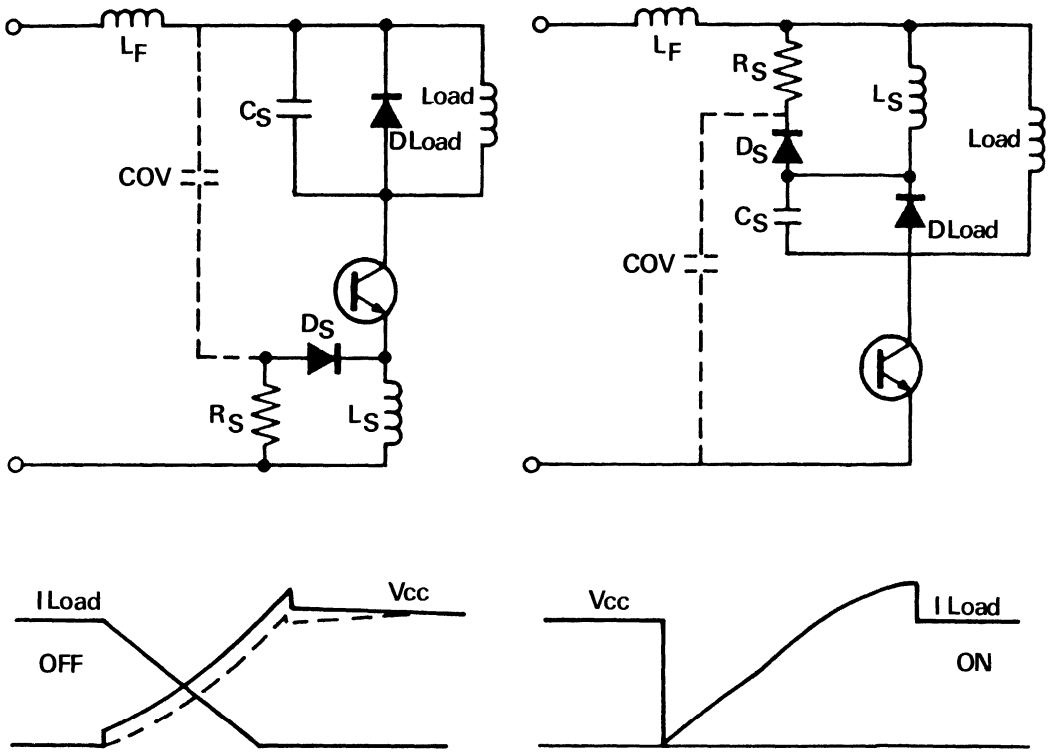


Figure 3-73 – Other common resistance snubbers

The advantage of both Figures 3-72 and 3-73 snubbers is that they diminish dv/dt during turn of (dotted line Figure 3-72).

F-3. Snubber for invertor leg

F-3.1. With turn off (shunt) snubber only

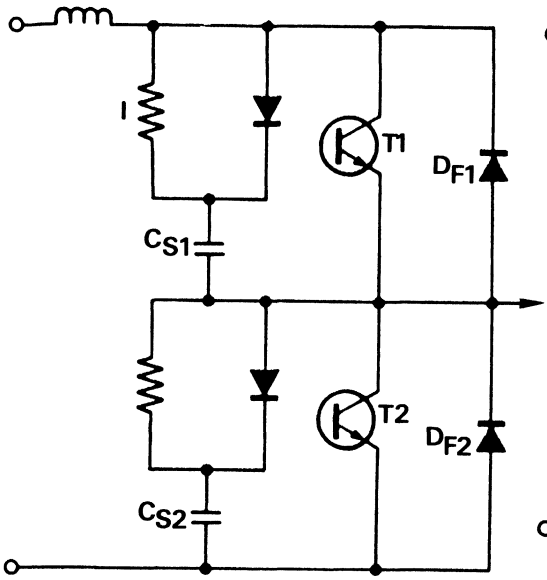


Figure 3-74 — Inverter leg turn off snubber

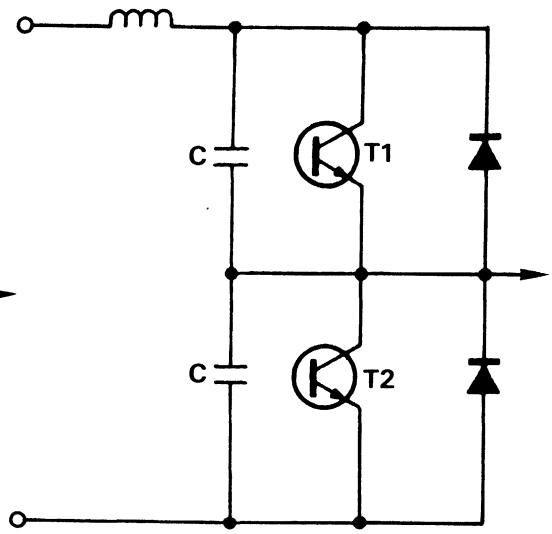


Figure 3-75 — Inverter leg turn off load line shaping

The first problem with this type of network is that during turn on the load current is diverted by the snubber.

Also, DF1 conducts when T2 turns on and CS1 charges thru T2, and CS2 will discharge in the same way.

So the turn on stress is very severe.

It is better to use the following arrangement with C = CS/2 in terms of turn on losses and for protection of the transistor.

The preceding table of switching losses gives the total sum of losses at turn on for the snubbing circuit which for the transistor is ET1 = 0,69 Vcc Iload t_f but we also have discharge due to the series transistor in the same leg so:

$$E_{T1} = 0{,}69\ V_{cc}\ I_{load}\ t_f + \frac{1}{2} V_{cc} (I_L + I_{rr})\ t_r \text{ if } I_{rr} = 0{,}3\ I_L \text{ and } t_r = t_f, \text{ we have:}$$

$$E_{T1} = 1{,}34\ V_{cc}\ I_{load}\ t_f$$
$$= 2{,}68\ K$$

K being losses without snubbing.

F-3.2. Complete snubbers (turn on and turn off)

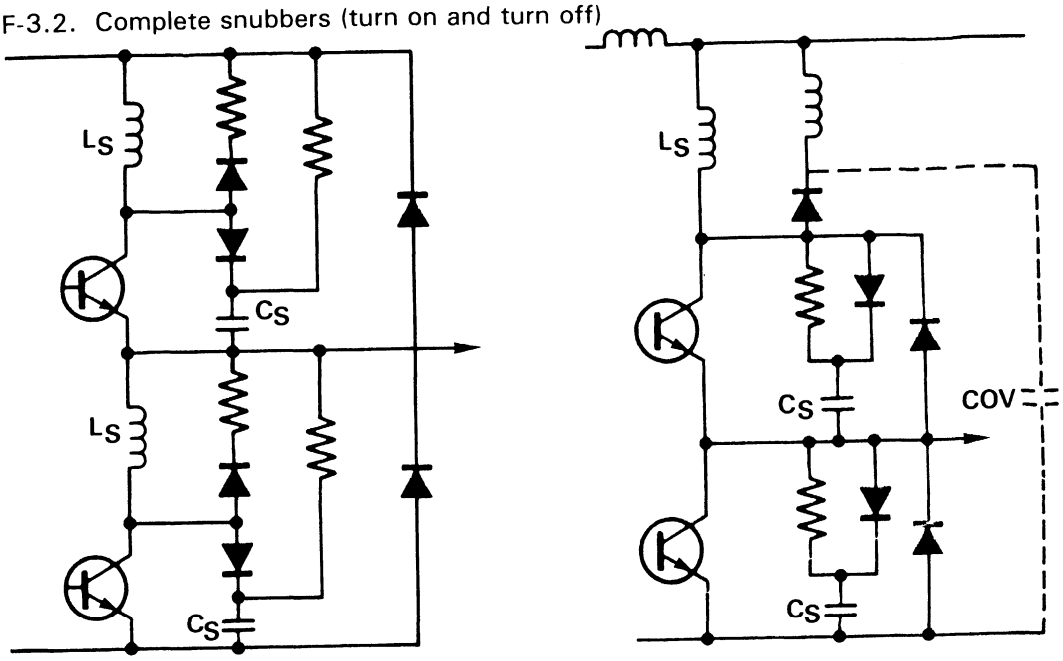


Figure 3-76 – Complete invertor leg networks

The main problem with this snubber is the oscillation of the circuit LS + 2CS at turn on of a transistor.

There is also latching of the inductance circuits by the freewheeling diode across the transistor.

These two circuits give the same results but in the case of Figure 3-76, dV/dt is limited on the freewheeling diode at turn off.

We can simplify the preceding circuits by using only one resistance.

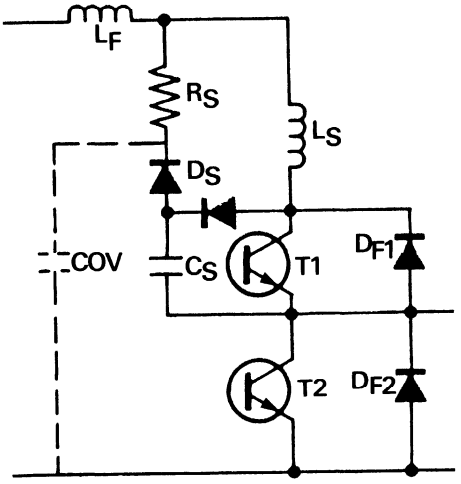


Figure 3-77 – Snubber with single resistance and capacity for invertor leg

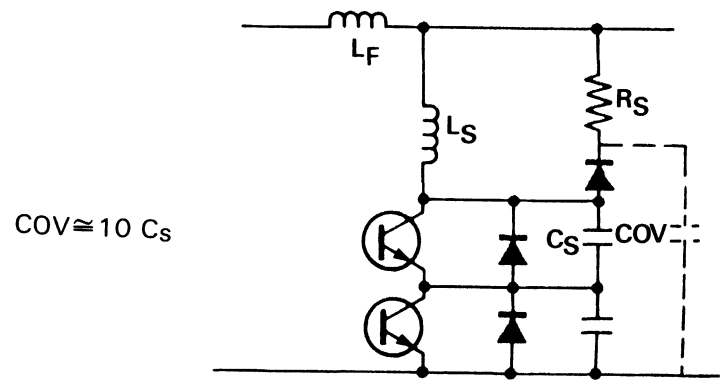


Figure 3-78 – Snubber with single resistance and 2 capacities for inverter leg

Ideally this has no turn on losses **and so we come to the ideal network for invertors with PWM.**

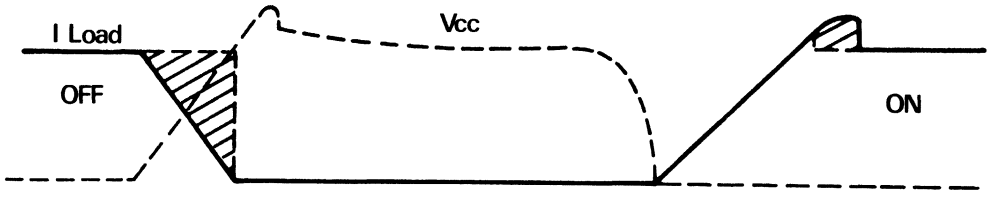


Figure 3-79

Turn on losses can be seen on preceding waveforms, i.e.:

$EON = 0{,}25\ CS\ Vcc^2 = 0{,}125\ Vcc\ IL\ t_f$ i.e. $\boxed{EON = \frac{K}{4}}$

Giving a reduction of losses of factor $2.68 \times 4 = 10.72$ or 9% of preceding losses (equation 8).

For multibranch convertors a single inductance can be used at turn on and a single resistance.

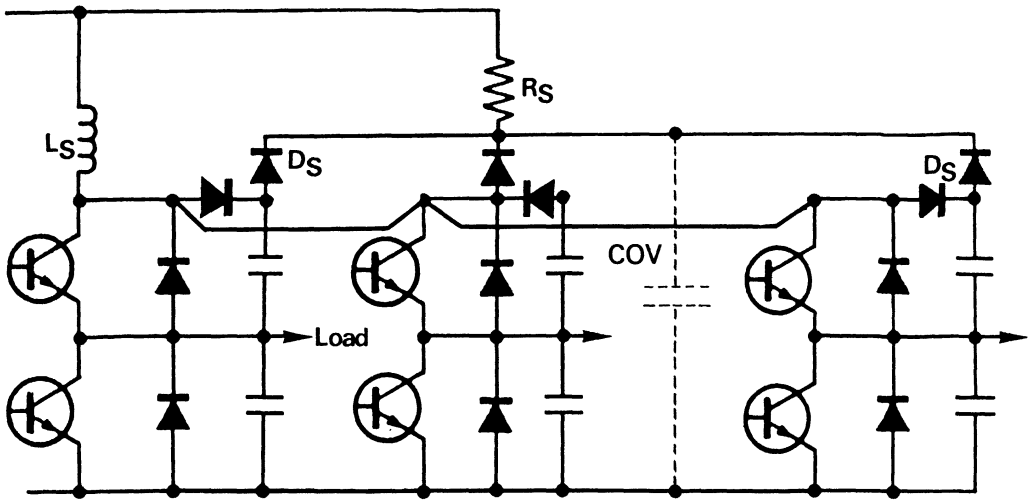


Figure 3-80 – Snubbers for three phase systems

The energy stored in the inductance at turn off is $E_{LS} = 0.5\ L_S\ I^2$ load this energy could be recovered with a transformer or a capacitance in place of RS and fed back to the source if possible.

F-4. Bibliography

(1) T.M. UNDERLAND – Snubbers for pulse width modulated bridge converters with power transistors or GTO's.
IPEC – Tokyo, 1983.

(2) W. McMURRAY – Selection of snubbers and clamps to optimize the design of transistor switching converters.
IEEE, 1980.

Choice of power switch

Section 4

TABLE OF CONTENTS

Choice of power switch

1. Introduction

The criteria for choosing power switch can be stated very simply: The device that provides the highest reliability within the confines of the application at lowest cost. However it is difficult to define the highest system reliability and it is even more difficult to take into account all the system costs: immediate costs and long term costs. We shall try to outline in more detail to give some simple guide lines for making the proper choice.

2. Reliability

Mathematicians define the reliability of an entity at the end of the "bath tub curve", excluding infantile mortality by the formula: $R(t) = e^{-\lambda t}$

λ expressing a certain number of failures in certain time period usually number of failures per hour.

For a group of components, the norm MIL-HOBK-2HB states that: λ system $= \Sigma \lambda i$

A) Influence of temperature

The preceeding laws are given at constant temperature: if these vary, ARRHENIUS gives an empirical formula that is back up by theoretical considerations: $\lambda = Ke^{-C/T}$

T being temperature in °K

K and C being constants dependent on material and temperature

From this law, a simple rule of thumb can be stated for silicon semiconductors:

λ **doubles for each increase of 10° C in junction temperature between 50 and 150° C**

B) Other influences

The environment has an important influence on reliability:

- potential
- power or temperature cycles
- humidity, corrosion
- fatigue, etc...

In the case of power switches, we can also consider:

- electrical field values and commuted currents
- the number and value of overloads sustained
- the number of working cycles (see figure 4-1)

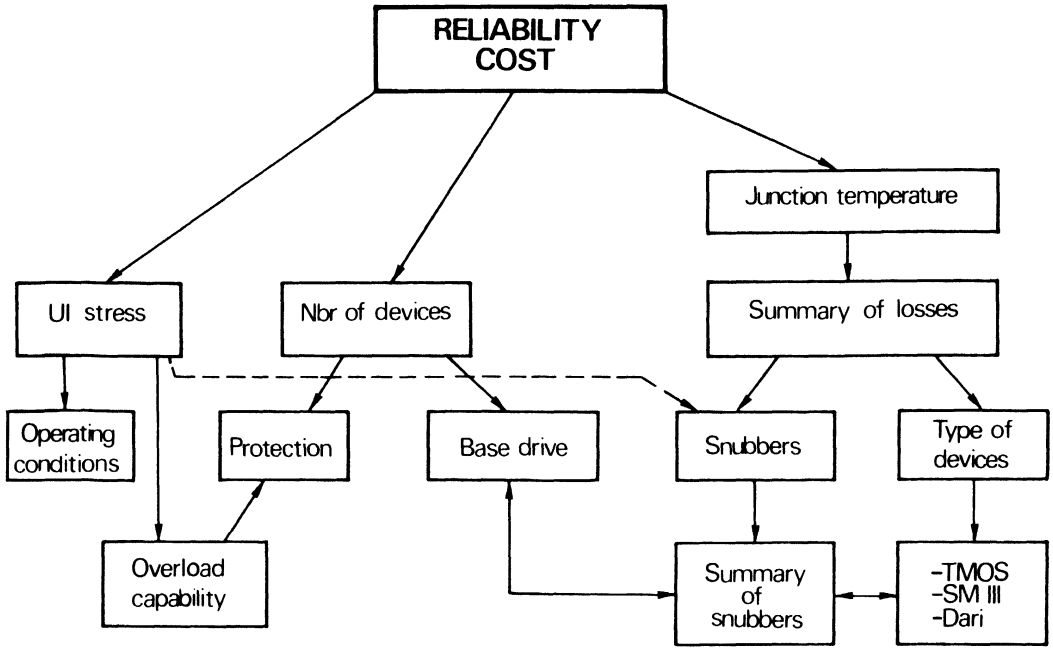


Figure 4-1

3. Costs

A) Short term costs

- analysis and development
- material, mounting, wiring
- passive components
- active components

Is the power switch is simple to use and mount, does it behaviour without complications so that the cost of analysis mounting and wiring are minimal.

Can the power switch operate fast to provide low junction temperatures with minimum control circuitry, can operating frequency be increased, the size of the system will be reduced, resulting in a reduction in direct costs. However, one must be very careful: when the frequency is increased – passive component costs increase: capacitors inductances, resistances.

Electro Magnetic Interference (EMI) will increase also and shielding will be required, which will add filters and special wiring thus increasing costs. There is, then, an optimum operating frequency according to type of application: as a first approximation an empirical formula for applications within 500 and 5000 W would be:

$F\ optimum = \frac{K}{\sqrt{Pout}}$ If we take $K = 10^6$, Σ Pout = 2500 W. The optimum frequency is

$F = \frac{10^6}{\sqrt{2500}} = 20KHz$ At Pout = 900 W: $F = \frac{10^6}{\sqrt{900}} = 33kHZ$

B) Long term costs

There are costs which are very difficult to determine but always underestimated: they depend the market place, its geographical area, sales network and technical support.

Also on the capability of the entire system: example, computer supplies.

To experience the maximum benefit with minimum long term cost we should try to by in the shaded area shown in Figure 4-2, the failure rates verses cost curve.

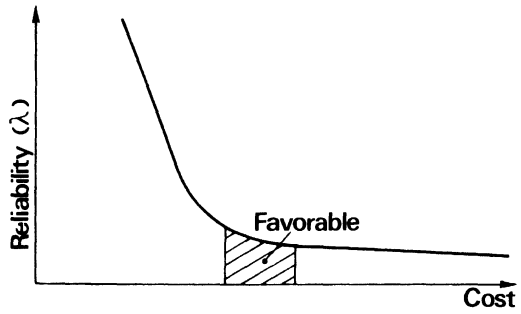


Figure 4-2 – Cost of an ensemble in relation to reliability

We shall now look at some aspects of power switches and their affects on reliability:

- stress
- number of components

4. Voltage current failures

Semiconductors can generally withstand very large current densities, if the current is evenly distributed over a large portion of the silicon.

Weaknesses occur as soon as we encounter concentrated electric fields.

They in effect distort the current flow and create high densities of localised current often in the region where there may be a molecular faults: i.e. dislocations, parasitic impurities, etc...

The most critical contributors to early failure are forwards bias safe operating areas (FBSOA) and the reverse bias safe operating areas (RBSOA). Operating devices near these limits especially a high voltages is the major cause of early high failures rates.

Fig. 4-3, shown the turn off and turn on waveforms that can represent many typical applications.

In this typical circuit, the device operates into maximum current and voltage during both turn-on and turn-off. If the load line is plotted on the SOA graph as shown in Figure 4-4, the maximum current-voltage conditions occur very close to the limit of the RBSOA curve. If a slight overload condition occurred right at turn-on or turn-off, a very dangerous situation could occur.

Worst yet, suppose there is a short-circuit, typically I_C will increase until a protection device detects the short and trys to turn-off the device. There would be then an I_C switched that could be double the normal I_C maximum, and we would thus have an overvoltage dV = L di/dt equal to twice the normal dV because L and dt are pratically constant as shown in Figure 4-4. The load line would cross the RBSOA curve and mostly destroy the device instantly, not because of the short circuit per se, but because the device would significant exceed its RBSOA capability during turn-off.

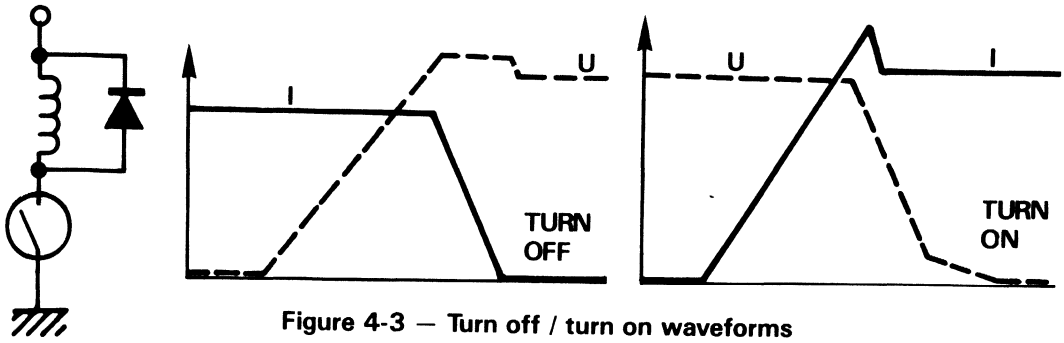


Figure 4-3 — Turn off / turn on waveforms

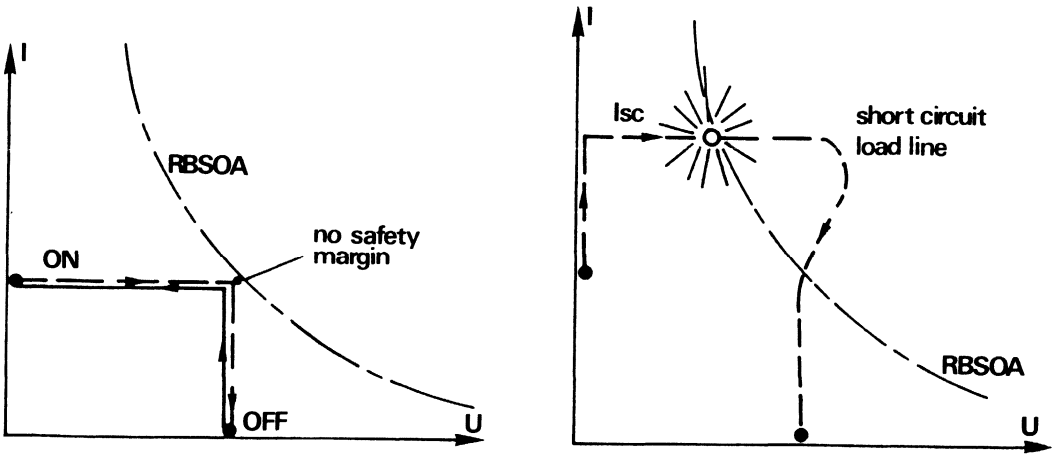


Figure 4-4 — Transient load lines

Therefore it is extremely important to check that the load line is a far away as possible from the RBSOA limits and if overload or short circuit conditions are possible consider:

- reaction time of the protection device Tp
- increase in load current during this time: $\frac{dI}{dt}$ max of circuit xTp
- overvoltage during turn-off $dV = L \frac{dI}{dt}$

In addition depending on the market conditions a comparison should be made of costs and added reliability due to:

- snubbing circuits
- or the use of more silicon.

As seen in Figure 4-1, snubbing networks can increase the reliability from two aspects:
- fatigue and
- junction temperature.

We shall see what the advantages are for:
- Guard banding and
- Improved reverse bias safe operating area for various kinds of products.

A) Guard Banding

With the RBSOA being mainly limited by voltage capability, designers tend to use higher voltage to provide the required guard band. However, by using the voltage guard band the can be a loss in gain and/or speed which can result in increase temperature.

Basic on experience, the best compromise is to use switching device at 0,8 Vcew. (see Figure 4-5).

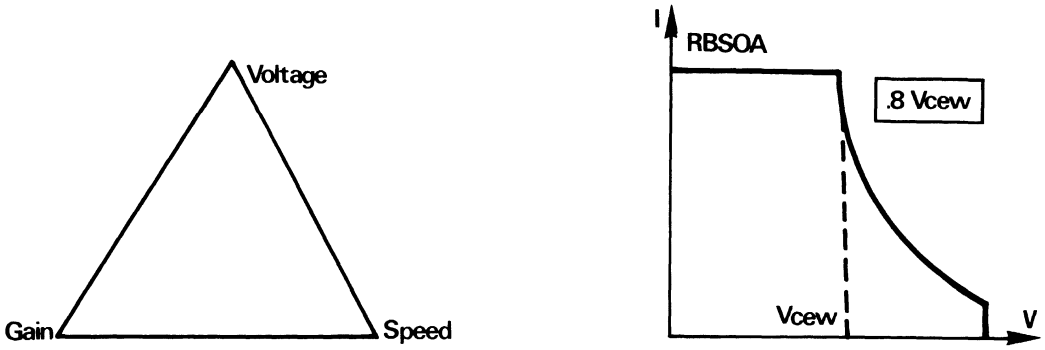


Figure 4-5 – Choice of breakdown voltage of a switching product vso and gain

B) Comparison of different switches verses RBSOA

In this section FETS and different bipolar technologies will be compared.

The RBSOA for various devices with the same silicon areas, are shown in Figure 4-6.

-A classic bipolar switching device switchmode 1, the MJE13009
-A bipolar Darlington switchmode 1, the BUT15
-A very fast switching bipolar switchmode III, the MJ16008
-A power MOS, the MTM8N40

It can be seen immediately that the bipolar devices virtually have identical safe operating areas for the same die area:
- in spite of the high speed of switchmode III
- even the Darlington, contrary to what is believed, does not have a lower safe operating area than other devices.

We also notice that the power MOS is no better that the bipolars for the same chip area, in fact the MOS device does not exhibit the extended voltage capability at low currents that is characteristic with bipolar devices.

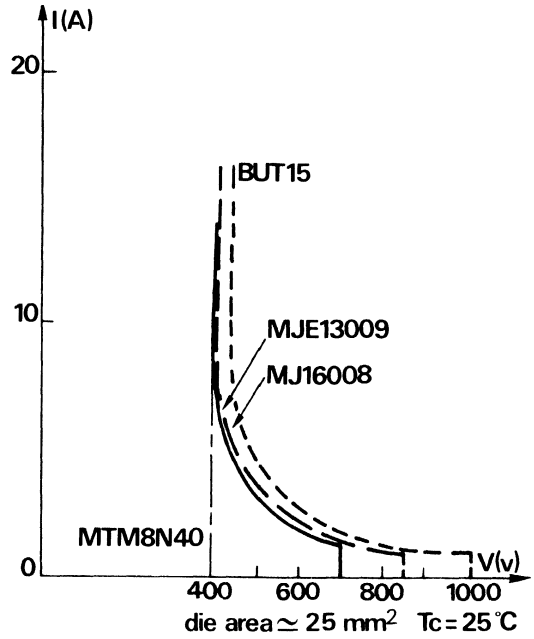


Figure 4-6 – RBSOA

C) Overloads

The power mosfets can support short circuit currents under nominal supply voltage for a period long enough for a protection device to work (about 20 microseconds) without affecting it's long term reliability, as long as the junction temperature stays below permitted maximum ratings.

For bipolar, this conditions is more of problem because the die is typically smaller for an equivalent voltage-current rating resulting in higher junction temperature for the same short circuits conditions.

Many manufacturers give overload limit curves based on maintaining the junction temperature at or below the rated temperature. Example: MJ10051.

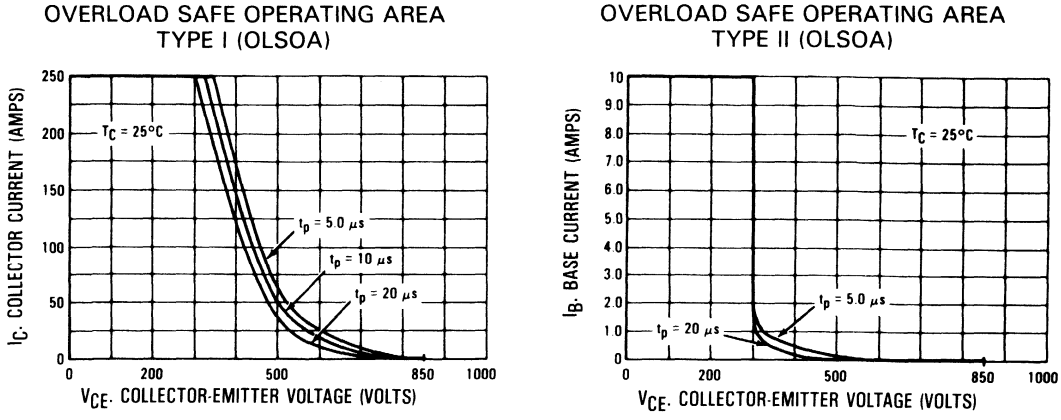


Figure 4-7 — Overload characteristics

To get an idea of junction temperature after short circuit and to understand why manufacturers limit the number of overloads possible without affecting the probable reliability of the device, the MJ10051 device with base drive of 2,5 A is used in a typical 420 Volt application, and the waveforms are shown in Figure 4-8.

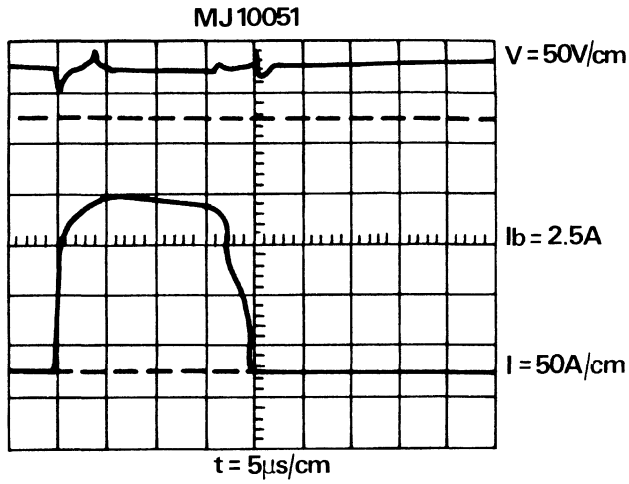


Figure 4-8 – Oscillogram of short circuit current

We see from these wavwforms that the short circuit current reaches 170 A ($\beta = 68$) for 20 microseconds defined by the turn-on time of a protection device.

To calculate junction temperature, Newell's formula can be used for short pulse =

$$T = \sqrt{\frac{4}{\pi}\frac{t}{k\rho c}}\ P/S$$

t : time in seconds
k: thermal conductibility of silicon: 0,85 W/cm. °C
ρ: silicon density: 2,3 g/cm³
c: specific silicon heat: 0,75 Joules/g. °C
P: power in Watts
S: useable area of chip in cm²
i.e. $T = 0{,}93\, t^{1/2}\ P/S$

The MJ10051 consists of 4 chips each of 40 mm² in parallel the active area of the emitter as 1,3 cm³, giving:

$$T = 0.93\ \ 10^{1/2}\ \ 10^{-6/2}\ \frac{600 \times 170}{1{,}3} \simeq 300\,°C$$

In looking closely at the short circuit current waveform, it can be seen that the current decreases with time and thus so does the junction temperature.

This phenomena can be explained by the gain curve in Figure 4-9, where we see that above critical current I*, gain decrease with temperature. Therefore the risk of experiencing excessive junction temperatures with the proper bipolar design is reduced.

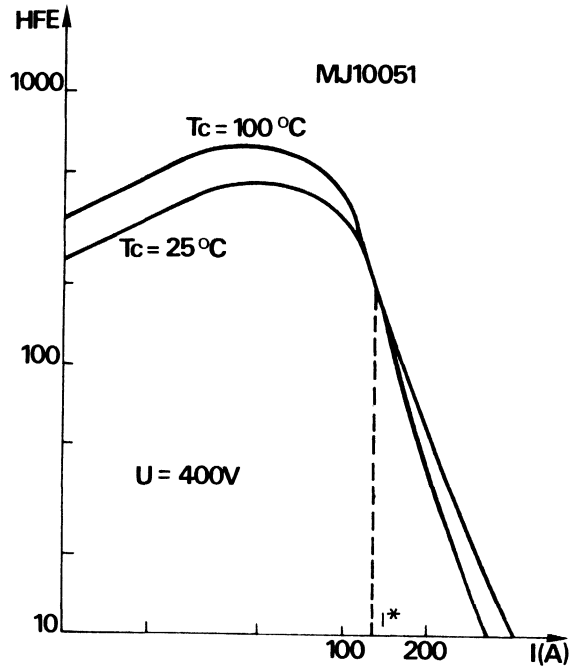


Figure 4-9 – Gain curve under nominal supply voltage and in temperature

5. Number of components

A) Control of any power switch

Control is easy if:

- the product needs only a weak control power. Good transfer: $\frac{Pout}{Pin}$
- The dIB/dt at turn off is not critical: drive loop impedance is weak giving good dV/dt.
- A negative supply is not obligation to obtain good turn off and weak losses.
- The variation in temperature of switching times is not excessive.

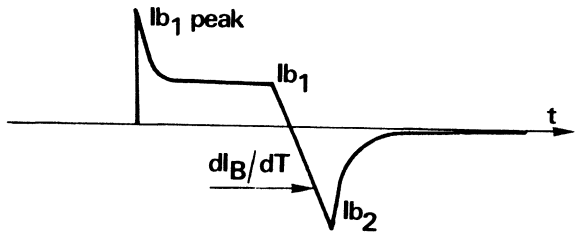


Figure 4-10 – Ideal base current waveform

For a bipolar devices, the typical base current waveform is shown Figure 4-10.

The Ib_1 peak is about equal to 3 times the Ib. This allows tfv and tvt voltage fall times to be as low as possible which reduces turn on losses.

Ib_1 must be as low as possible, while still maintaining quasisat, so that tc and ts turn off times are as low as possible.

The following table shows the effects of these different parameters on various types of power switches. This information also indicates that the device that are the easiest to control are, in order:

- the power MOSFET
- the switchmode III
- the standard Darlington

Table 4-1

	Without I_{b1} peak		With I_{b1} peak		dIB/oit limit		T = 100°C – 5V		TC = 100°C	
	tfv nS	tvt µs	tfv ns	tvt µs	L_b µH	A/µs	tc ns	ts µs	tc µs	ts µs
D.H.V. MJ8504 sm I	900	8	500	6	4	1	500	5	1.5	7
D.M.V. BUS48 Sm II	220	4	120	3	1	4	100	2	.4	4
D.M.V. MJ16010 Sm III	230	4	120	3	.2	12	50	1	.2	4
Dari BUT15 Sm I	800	6	400	4	1	5	400	2	1.5	4
Dari MJ10051 HCP	800	5	400	3.5	4	1	1000	10	3	10
MOSfet MV I5N40	150	1	100	1	–	–	50	.1	.1	.1

To illustrate this conclusion, Figure 4-11, shows 2 kinds of control from CMOS logic:

- one for switchmode 1 products, darlingtons and discretes
- one for switchmode III and MOS products

Control of the fast devices is simple and does not require negative off bias.

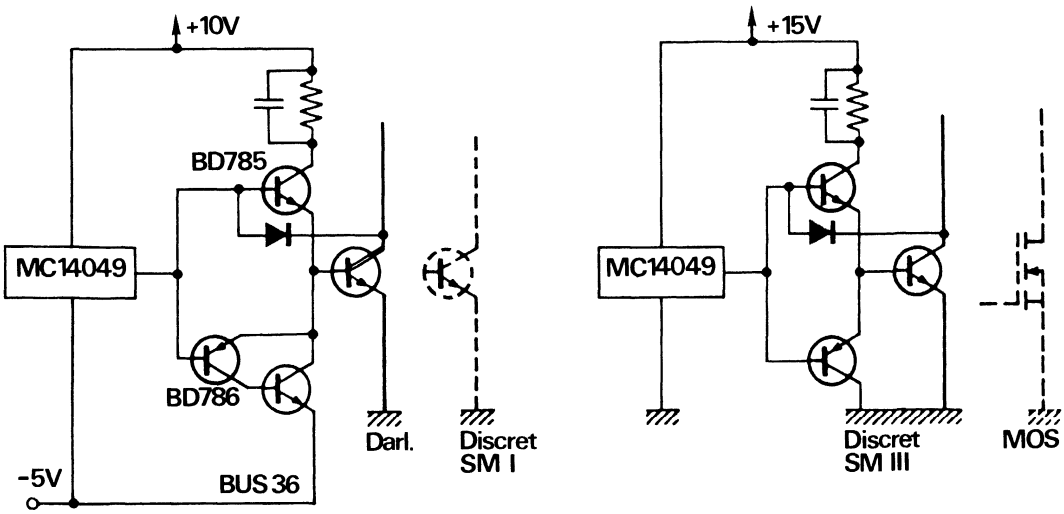


Figure 4-11 – Control circuits for different power switches

B) Protection

It is clear that power MOSfets, which typically have more silicon than an equivalently rated bipolar, can support high short circuit currents (see previous paragraph), so short circuit protection by current detection (i.e. resistance, transformer) is usually sufficient.

On the other hand, these products are highly sensitive to overvoltage and should have transient suppressors (power zeners) between drain and source and between gate and source.

High power bipolar products are limited in withstanding short circuit conditions. They must therefore be protected quickly (dIc/dt) and efficently with saturation detection (VCEsat) and by detection of base voltage VBEsat (faster). Overvoltage protection can be accomplished with snubbing circuits which will be looked at later.

6. Junction temperature verses switching losses

This is definitely the most important parameter for reliability. Losses must first be locked at.

A) Conduction losses

For bipolars, simply take the VCEsat of forced gain and predicted load current with the cyclic relation we get:

$$\text{ON losses: } V_{CEsat} \times I_{sat} \times \delta$$

For power MOSfets, we take RdSon 25° in the manufacturers data sheet, multiply by 1,8 to get Rdson 100° and we have:

$$\text{ON losses: } R_{dSon} \times 1{,}8 \times I_{sat}^2 \times \delta$$

B) Switching losses

B-1. – At turn on losses

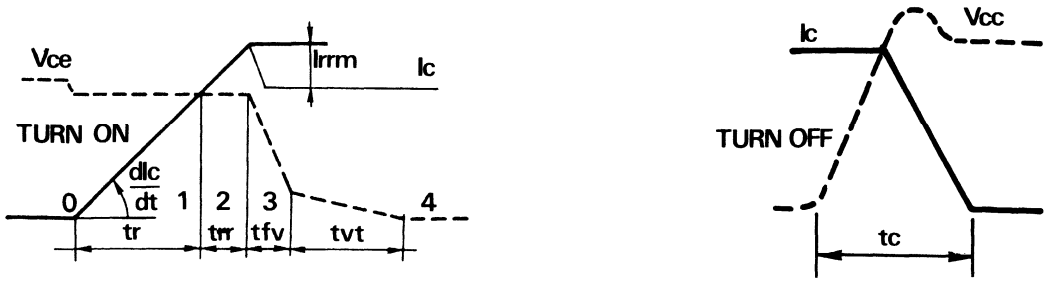


Figure 4-12 – Current × voltage waveforms at turn on and turn off

The diagram of Figure 4-12 gives the general shape of current and of voltage at turn on and turn off.

Irrm being the maximum freewheeling diode reverse current measured nominal with the working current and with the turn off slope given by the power switch.

Losses can be broken down into 3 parts:

1) The current rise up to Ic + Irrm gives $Won,2 = \frac{1}{2}$ (Ic + Irrm) (tr + Trr)

or $= \frac{1}{2}$ (Ic + Irrm) $(\frac{Ic + Irrm}{dIc/dt})$

$Won,2 = \frac{1}{2}$ Vcc $\frac{(IC + Irrm)^2}{dIC/dt}$

with a fast freewheeling diode we can take the worst case as Irrm = 0,3 Ic giving

$Won,2 = \frac{1}{2}$ Vcc $\frac{(1,3\ Ic)^2}{dI/dt}$

2) Fast drop in tfv voltage $Won,3 = \frac{1}{2}$ Vcc Ic tfv

3) Slow desaturation of tvt voltage $Won,4 = \frac{1}{2}$ (0,1 Vcc) Ic tvt

If we take tvt of 10% to 2% of Vcc

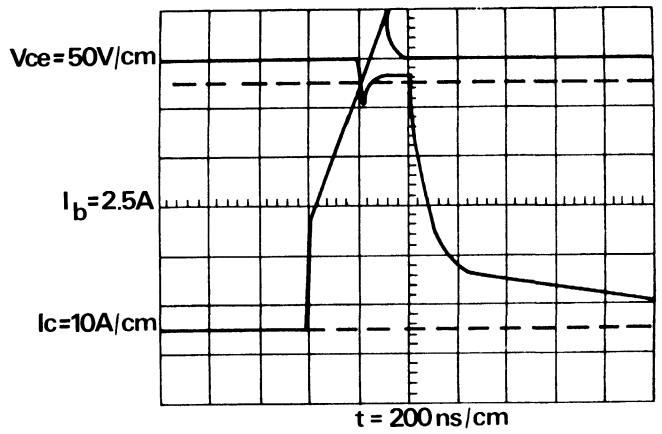


Figure 4-13 – Turn on / MJ10051

The waveforms in Figure 4-13, show the different losses. Usually, Won,3 and Won,4 represent about 90% of the total losses at turn on. So the influence of trr of the free-wheel diode and that of dIc/dt of the switch are relatively unimportant for turn on losses.

Won,2 losses are dependent on the current rate of rise rate at turn on: dIc/dt. The waveforms for different devices in the same package and stiff on control, are shown in Figure 4-14.

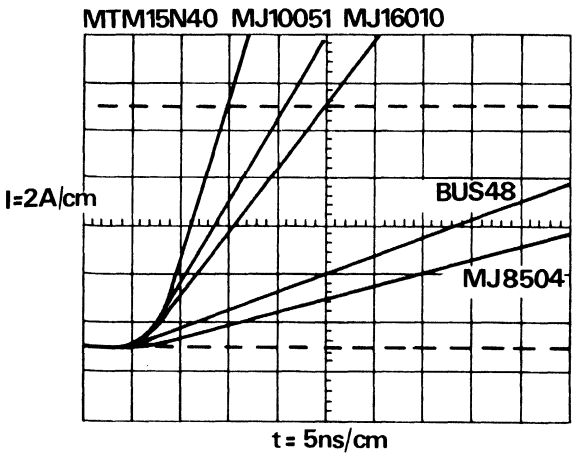


Figure 4-14 — dI Switch/dt at turn on

From these waveforms:

TABLE 4-2

A/μs	dIc/dt
MJ8504	100
BUS48	150
MJ16010	500
Darlington MJ10051	600
MOSfet 15N40	1500

B.2. – Turn off losses

Cross over time refers to the crossover time of voltage and current at turn off:

$$WOFF,\ F = \frac{1}{2}\ Vcc\ I.load.tc$$

B.3. – Summary of losses – Conclusions

The losses are summarized according to type of power device in table 4-3, in which the silicon area per device is also shown, and the useful power of the device equals $V_{cew} \times Isat$.
The silicon efficiency is given in W/mm².

Table 4-3

	Die area mm²	Use full power kw	Efficiency w/mm²	Won 100°C mJ	Woff 100°C mJ	On losses δ=.5 w	Losses 10 kHz w	Losses 100 khz w	Losses 10 P 10^{-3}	Losses 100 P 10^{-3}
MJ8504	35	3	86	2.9	.75	2	39	372	13	125
BUS48	35	4.5	130	2.2	.45	4	31	274	7	61
MJ16010	40	3	75	1.1	.075	2	14	122	5	41
BUT15	27	6	220	5	1	15	75	615	12	102
MJ10051	160	30	187	23	30	40	573	5340	19	180
MOSfet 15N40	50	4.5	56	.52	.07	45	51	104	11	23

Table 4-3 shows some interesting facts:
- the efficiency of silicon for Darlingtons is high

- that total losses at 100 KHz for the bipolar switchmode III and power MOSfet are practically identical
- that switching losses increase rapidily whatever the device type and case, when frequency increases

Clearly switching improvement systems are indispensable when control power becomes great (> 500 W) and/or the work frequency increases the losses in the switch itself significantly.

7. Switching improvement circuits – Snubbers

Not only do these circuits allow power switches to control high power or increase working frequency, but they also reduce current voltage/RBSOA fatigue as we saw in chapter 4.

The following compromise should now be studied:

- increase of total λ due to additional components
- reduction of λ for the switch by 2 with each reduction in junction temperature of 10°
- reduction of λ for the switch by increasing safety coefficient: load line in the safe operating area at turn on and turn-off
- From the work of Norvegian professor Tore M. Underland, of the University of Tronheim, the diagram in Figure 4-15, shows one of the best subbing circuits in terms of performance improvement/simplicity (cost) for an invertor leg

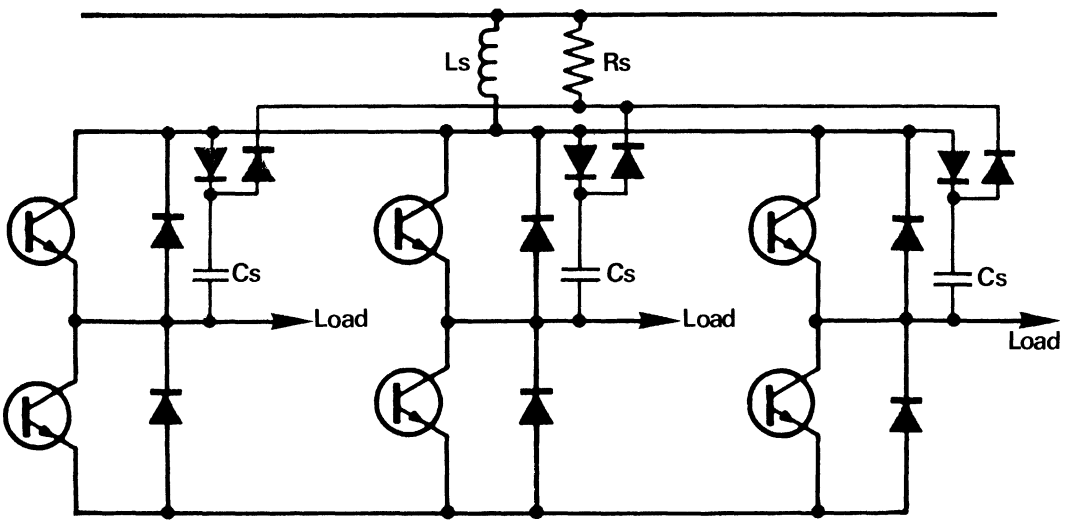


Figure 4-15 – Snubbing circuit for a three phase switch

This snubbing network result in:

A) complete elimination of turn off losses [(.5 Vcc Ic tf) without the snubbing circuit]

B) Reduction of turn on losses per switch to: Won,T = .125 Vcc Ic tr instead of .5 Vcc Ic tr without the snubbing circuit.

C) It also has the advantage of reducing the dV/dt voltage on the Vdf freewheeling diodes at turn on (Figure 4-16).

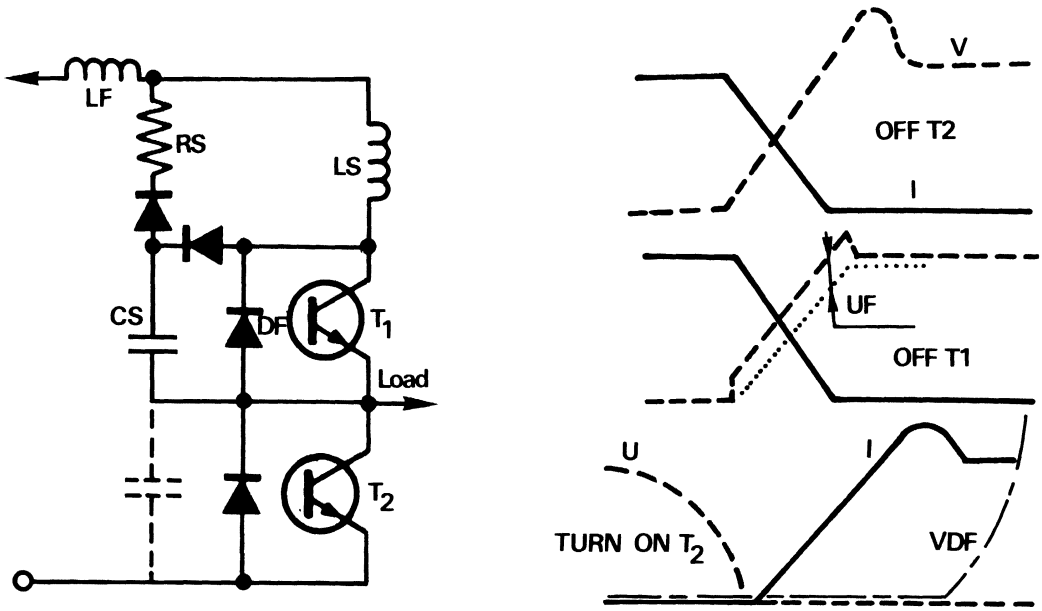


Figure 4-16 – Oscillogram of each switch and voltage gradient on freewheeling diode

D) Disadvantages:

- an overcurrent at turn on
- an overvoltage at turn off

At turn on if the Irrm of the freewheeling diode is equal to about 0,3 Iload and the snubbing network inductance is equal to $Ls = \frac{3\ Vce}{2\ I\ load}$ tr and tr = tf, we have an overcurrent I = 0,7 Iload which is quite easily supported by a semiconductor power switch with very low voltage acrossed its terminals (see RBSOA or OLSOA).

The snubbing network capacitance could be reduced which would reduce this overcurrent, but this would increase the overvoltage at turn off which could be more dangerous for the switch

$$\text{overvoltage} = I\sqrt{\frac{LF}{Cs}}$$

At turn off, if the parasitic inductance of the LF wiring is relatively low LF ≦ 0,1 Vce tf/I load. The overvoltage is roughly equal to Δ Vcc = 0,4 Vce for the transistor at a zero load current: I load = 0. If LF = 100 nH and a switchmode III MJ16010 is used with a tf of 50 ns then the overvoltage is: Vce = LF Ic/tf = 10^{-7} 10/510^{-8} = 20 V.

E) Table 4-4 shows a comparison of losses with and without a snubbing circuit.

Table 4-4 – Snubbing Network

	Cs nF	Ls µH	RS	Losses in RS mJ	Switching losses without snubbing mJ	Switching losses with snubbing mJ
BUS48	5	6	10	0,45	2,65	0,06
MJ16010	1	1	1,5	0,15	1,18	0,02
BUT15	10	7	7,5	0,8	6	0,15
MJ10051	40	18	6	15	53	4

The reduction in switching losses are very considerable (> 90%) but there are also significant improvements in junction temperature, (i.e. of the λ). To calculated the junction temperature before and after snubbing the case to heat shink thermal resistance of a TO3 = 1° C/W and chip to case $R\theta$ jc = 0,25°C/W, was used. The devices were mounted on a thermal heat sink with the ambient temperature at 60°C.

Giving the following table:

Table 4-5 – Changes in junction temperature

	10KHz Total losses (W)		Junction temperature °C		λ
	without snubber	with snubber	without snubber	with snubber	Improvement
BUS48	31	4,6	122	70	$2^5 = 32$
MJ16010	14	2,2	88	65	3
BUT15	75	17	210	94	5000
MJ10051	573	80	346	100	

The preceeding table only gives improvement of λ in terms of temperature, but the snubbing network also reduces the susceptibility to thermal fatigue and increases the margin of safety of the application: these improvements are difficult to quantify but they can be considered in terms of 100 for the λ.

If we total up the advantages introduced by the snubbing circuit, we should also add up those additional components required for this circuit:

- one capacitor
- two diodes
- one half-resistor and inductor for an invertor leg, 1/4 for a bridge, 1/6 for an 3∅ convertor.

We can say then at first estimate that the whole λ = λ switch + λ network so whole λ = 10 λ switch, giving the following table: Table 4-6.

It seems from the evidence that the snubbing networks are always profitable in terms of probable lifetime.

Table 4-6

	λ Improvement in Tj	λ Improvement in stresses	λ Losses for the total system	λ Improvement TOTAL
BUS48	32	100	10	300
MJ16010	3	100	10	30
BUT15	> 5000	100	10	50
MJ10051	∝	100	10	∝

F) An example of the size and costs of a snubbing circuit in relationship to the type of switch.

The formula's for the elements of the snubbing circuit are:

$CS = 1/2\ I/V\ tf$ $LS = 1/2\ V/I\ tr$ $RS = 0{,}3\ V/I$ or $\frac{2}{3}\sqrt{\frac{Ls}{Cs}}$ losses in RS are $WRS = 1/4\ VItf + 1/4\ VI\ tr$

demonstrate immediately that the fastest devices: low tf and tr, have low component values, thus low in cost, small in size and low losses in Rs making for greater efficiency overall.

For example using the MJ10051 Darlington switchmode 1 device and a discrete Darlington constructed with switchmode III devices: an MJ16010 driving 3 other MJ16010 in parallel representing the same silicon area, as the MJ10051, the following information was calculated for each.

Table 4-7

	MJ10051	4 x MJ16010
CS nF	40	4
LS μH	18	1
Losses in RS mJ	15	.6

8. Types of power switch

We have already seen in previous chapters that the characteristics of power products influence the reliability of the system in which they are mounted:

- by their safe operating areas
- by their overload possibilities
- by their control
- by their speed

We shall now look at each family of products and give their main advantages in terms of total reliability.

A) Power MOSfets

They have great overload capability.

They are very fast and that their control power capability $\frac{Pout}{Pin}$ is large.

It remains that for medium and high voltages the Rdson is important and temperature variation also important.

The cost of products with medium and high voltage capability are higher than their bipolar equivalents (see Figure 4-17).

But for low voltage MOS (< 200 V) the RdSon is low enough to produce equivalent on state voltage compare to bipolars and will be improved in the coming years so costs will drop below corresponding bipolars (see Figure 4-17). Finally, the variation of RdSon in T° for low voltage MOS is less than for high voltage MOS.

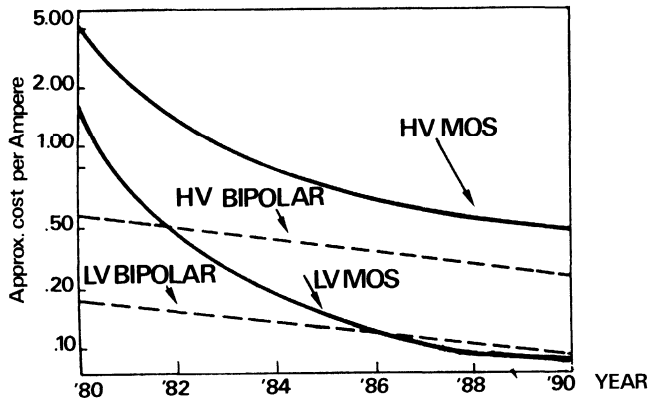


Figure 4-17 – Estimated cost projection of power bipolar and MOS transistors

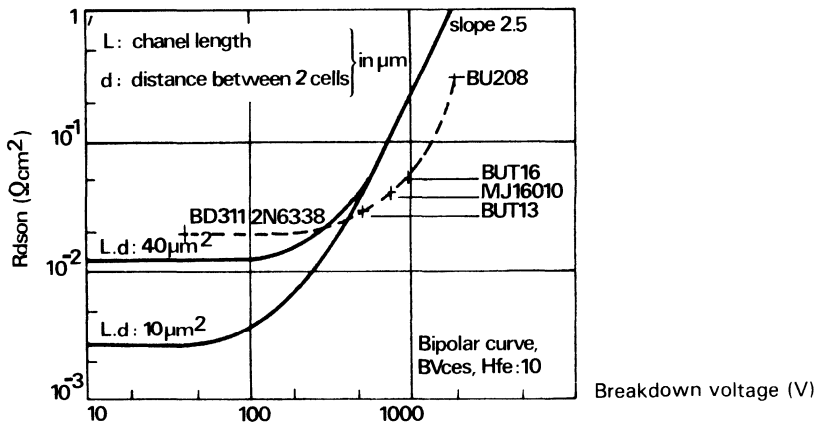
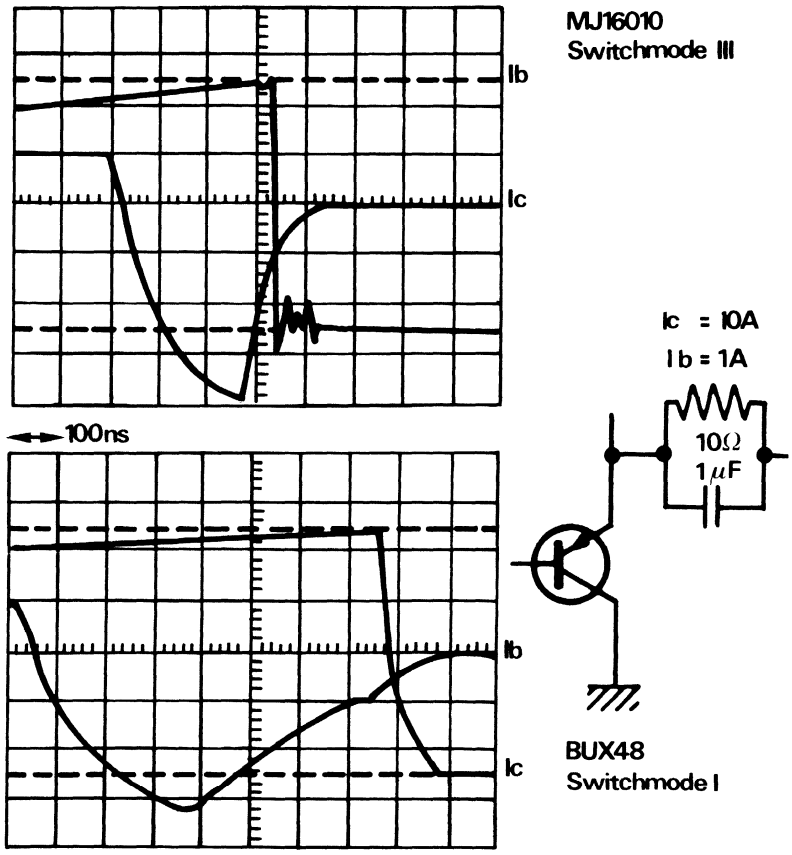


Figure 4-18 – Rdson versus BVdss

B) Switchmode III bipolars

These hollow emitter devices with fine geometry have very high switching speeds: more or less similar to high voltage power MOSfets. They require only simple control to obtain these speeds (see Figure 4-11) temperature variation of switching times is far less than that of the older switchmode 1 bipolars.

To illustrate the difference in switching times obtained with the same base drive Figure 4-13, compares the turn off of a BUX48 and a switchmode III.



* Motorola has stopped manufacturing of this product; it has been replaced by the BUS48.

Figure 4-19 – Switchmode I/III comparison

For medium frequency (20 – 50 KHz), by replacement of the older switchmode 1 with switchmode III losses can be reduced by a factor of 2.

Table 4-7

	ts(ns)	t_f (ns)	Total losses 10 KHZ (W)
BUX48	1000	200	20
MJ16010	500	50	12,5

Reliability is also improved in similar proportion.

For high frequency(50-100kHz)applications there are also advantages in relation to the power MOSfet. To illustrate these advantages, we have compared the relative losses of all the technologies in terms of frequency and case temperature in Figure 4-20.

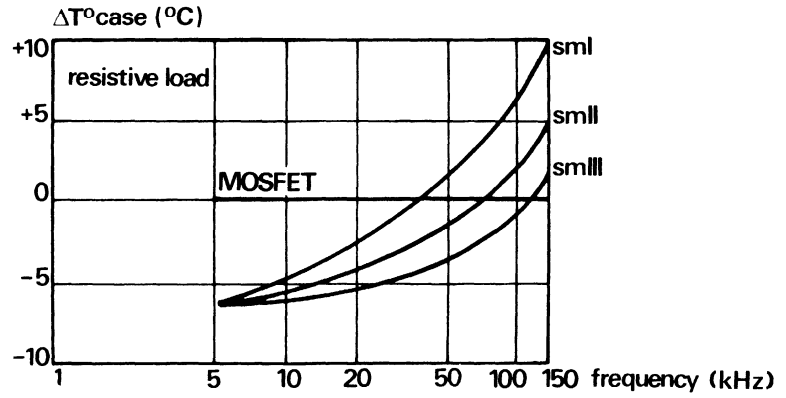


Figure 4-20 – Comparison of losses in relation to frequency for 4 types of power switches

C) The Darlington

The silicon efficiency of integrated Darlingtons is good (see Table 4-3 power/area).

These products have very good dIc/dt during turn on: (see Figure 4-14).

Paralleling is easier than with discrete bipolar products since:

a) The VBEon variations in production is less $\approx \pm 10\%$ instead of $\pm 15\%$ for discrete devices.

b) The Darlington is a natural Baker clamp, so that variations in storage times with temperature are much lower.

Protection against short circuits by detection of VBEsat variation is easier with the Darlingtons.

The Darlington is as strong as the other devices (see Figure 4-6).

For all these reasons, the Darlington is recommended for high voltage, high current applications since it is the only device with high gain, good switching and a good SOA capability.

9. The cases – Paralleling

If we look at comparative costs of packaging, mounting of passive components and semiconductors for a given application and their evolution over a period of time (Figure 4-21), we see that the mounting – wiring – packaging cost becomes more and more predominant, in the total cost picture.

So it is clear that packages with easier assembly capability than that of the traditional (TO 3) can be a significant improvement in total costs.

It is also evident that easier assembly means less chance of failure in the long term (improvement of λ).

Paralleling of case TO 3 is a costly operation in terms of mounting, worst case analysis and reliable. So packages which eliminate the paralleling required for high power application also improve the quality/cost (see Figure 4-22).

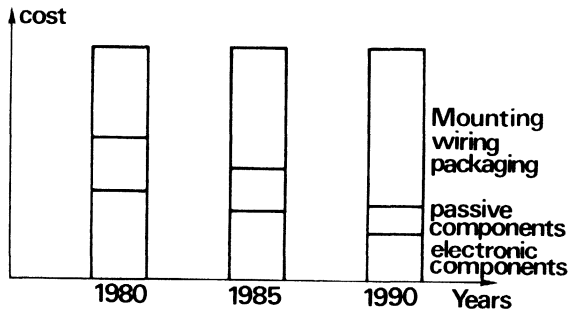


Figure 4-21 – Cost distribution tendencies for one application

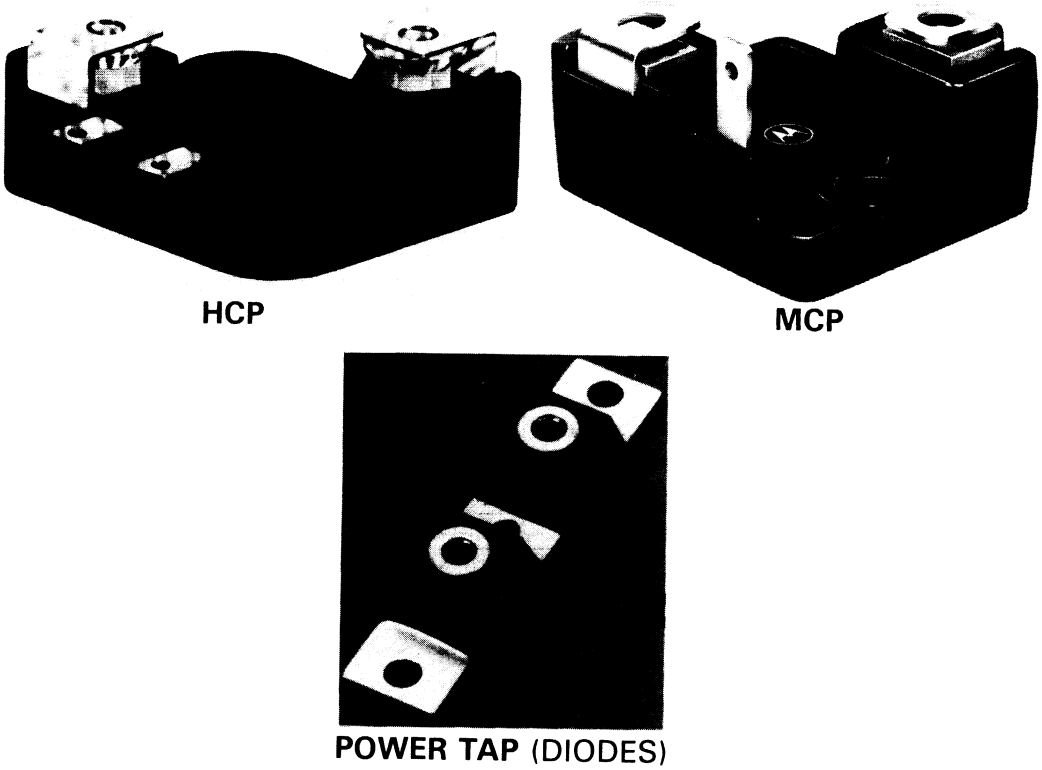


Figure 4-22 – New packages for medium power range components

10. Conclusions

We have seen that the junction temperature is a primary parameter governing reliability thus it is important to keep switching and on losses to a minimum.

It appears that switching improvement circuits are necessary for medium and high power applications and that they are profitable in terms of:

$$\frac{\text{reliability improvement}}{\text{supplementary costs}}$$

Fast products are preferable because losses are reduced but also because size, costs and assembly times can be reduced when operating at higher frequencies.

Devices which only need a few components around them in order to function properly are always advantageous from both a reliability and cost of component standpoint.

The above can be summarized in a table showing switching power value or frequency used verses

$$\frac{\text{quality}}{\text{cost}} \text{ ratio}$$

The limits given are variable and may change according to each particular case.

Table 4-8

Application domains			Best switches for good ratio: quality/cost
U	F	P	
≤200 V	From C.C. to 200 KHZ	<1 KW	Power MOSfet
		>1 KW	Bipolar transistor with low V_{cesat} - Power MOSfet in MCP/MCP
200<U<500 V	F<10 KHZ	<5 KW	SCR (GTO-TRIAC) – GEMFET – Bipolar – TMOS
	F>10 KHZ		Bipolar, smII/III, TMOS according to the application volume
500<U<2000 V	F<1 KHZ	<50 KW	SCR – GTO – TRIAC – GEMFET – Bipolar
	F<10 KHZ		Bipolar, smI/II, Darlington TMOS for P<200 W
	F≤100 KHZ		Bipolar, smIII, Darlington TMOS for P<200 W
	1<F<10 KHZ	50<P<500 KW	Bipolar, Darlington, smII/III GTO, GEM, ASCR
U>2000 V	F<1 KHZ	P<1 KW	Series mountings of TMOS or Bipolar
		P>5 KW	SCR, ASCR, GTO